

SiC-MOSFET module Application Manual

Minebea Power Semiconductor Device Incorporated

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so that you can refer to it at any time.

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SAFETY PRECAUTIONS

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Safety-related precautions are indicated by the headings shown below. These are combinations of safety warning symbols and the headings "Danger," "Warning," "Caution," and "Notice."



This is a safety warning symbol. It is used to alert you to potential hazards that could cause harm to people. To avoid possible injury or death, follow the safety messages that accompany this symbol.



Danger : Indicates a hazardous situation which, if not avoided, will result in death or serious injury.



Warning : Indicates a hazardous situation which, if not avoided, could result in death or serious injury.



Caution : Indicates a hazardous situation which, if not avoided, could result in minor or moderate injury.

Notice : Indicates information considered important, but not hazard-related (e.g., messages relating to property damage).

※Serious injuries mentioned above refer to those that result in lasting effects such as blindness, wounds, burns (high or low temperature), electric shock, fractures, poisoning, and those requiring hospitalization or long-term outpatient care for treatment. Moderate or minor injuries refer to injuries, burns, electric shock injuries, etc., that do not require hospitalization or long-term outpatient treatment. Non-personal injuries refer to damage unrelated to personal injury, such as property damage, product malfunction or breakage, data loss, and other non-personal injury-related damages.

SAFETY PRECAUTIONS

< Common Safety Precautions >

- When designing electronic circuits, please ensure that the device is used within the specified "Absolute Maximum Ratings" under any variations in external condition changes (within the guaranteed range). Additionally, for pulse applications, ensure that the ratings do not exceed the "Safe Operation Area (SOA)."
- Semiconductor products may experience malfunctions or failures with a certain probability. Therefore, please give sufficient consideration to safety design, such as redundancy and malfunction prevention, to prevent the expansion of damage in the event of a failure.
- When using the product, be sure to contact MPSD and obtain prior written approval. If you have any questions, please inquire at our sales office.
- Perform actual load tests that cover the conditions of current, voltage, frequency, pulse width, etc., that may occur in actual application.
- SiC-MOSFET modules integrated into power conversion systems, such as inverters, undergo repeated temperature fluctuations due to self-heating caused by power dissipation. These temperature variations subject the SiC-MOSFET modules to thermal stress. Ensure that the modules are operated under conditions where the SiC-MOSFET module lifetime limited by thermal stress is equal to or longer than the designed service life of the equipment. For further details, please refer to Section 3-5-5, "Concept of Power Cycle Lifetime in Actual Equipment".

SAFETY PRECAUTIONS

The following warning labels are related to semiconductor devices. Failure to comply with these warning labels may result in a risk of death or serious injury. Please note that the order of this list does not indicate the order of importance. Each item is equally important.

 Warning	Page
(7-1-1. Warning regarding package rupture) ● In the event of a load short-circuit or arm short-circuit, turn off the SiC-MOSFET module within a short duration (approximately several μ s). Failure to do so may result in package rupture.	7-1
(7-1-2. Warnings regarding burns and electric shock) ● Do not touch or approach while it is energized. There is a risk of burns or electric shock.	7-1

SAFETY PRECAUTIONS

The following caution labels are related to semiconductor devices. Failure to comply with these caution labels may result in minor injury or material damage only. Please note that the order of this list does not indicate the order of importance. Each item is equally important.

 Caution	Page
(Chapter 2. Specification Details) ●When designing electronic circuits using semiconductor devices, ensure that the specified 'absolute maximum ratings' of the device are not exceeded under any external condition changes. Additionally, for pulse applications, ensure that the ratings of the 'safe operation area (RBSOA/RRSOA)' are not exceeded.	2-1
(7-2. Cautionary Notes) ●After SiC-MOSFET failure, ensure that short-circuit current does not flow for an extended period (approximately several hundred microseconds). There is a risk of smoke generation or fire.	7-1

CAUTION

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<About RoHS>

The RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment) Directive is a regulation on hazardous substances enforced by the EU (European Union) on July 1, 2006. It prohibits the inclusion of specific hazardous substances in electrical and electronic equipment.

Currently, the regulated substances are lead (Pb), cadmium (Cd), hexavalent chromium (Cr⁶⁺), mercury (Hg), polybrominated biphenyls (PBB), polybrominated diphenyl ethers (PBDE), bis(2-ethylhexyl) phthalate (DEHP), benzyl butyl phthalate (BBP), dibutyl phthalate (DBP), and diisobutyl phthalate (DIBP).

Regarding the regulatory concentration (threshold), cadmium is limited to a mass fraction of 0.01 % (100 ppm), while all other prohibited substances are limited to a mass fraction of 0.1 % (1000 ppm). Products containing these 10 substances above the threshold (0.01 % for Cd, 0.1 % for others) cannot be sold within the EU. However, exemptions are granted for applications where technical substitution is difficult.

In relation to RoHS compliance for SiC-MOSFET modules, lead (Pb) contained in the solder used to connect the chips to the DCB substrate is particularly relevant. For information on the RoHS compliance status of our SiC-MOSFET modules, please refer to the status list published on our website.

REVISION HISTORY

Rev. No.	History (revision and reasons)	yy.mm.dd	Reported	Checked	Approved	Rev. No.
Rev.0	New	2026.03.13	Tanimura	Sakurai	Inaba	Rev.0

PREFACE

This instruction manual provides specifications, main characteristics, various design guidelines (gate circuits, heat dissipation, protection circuits), and precautions for the use of SiC-MOSFET modules.

The contents of this instruction manual are subject to change without notice due to revisions and updates. For the latest information (detailed specifications and applications for each product), please refer to our website (<https://www.minebea-psd.com>).
If you have any questions, please contact our sales office listed below.

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Explanation of Terms and Abbreviations

For the terms and abbreviations used in this instruction manual, please refer to the table below.

Terms/abbreviations	Original word
SiC	Silicon Carbide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
DCB	Direct Copper Bonding
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
SBD	Schottky Barrier Diode
REACH	Registration, Evaluation, Authorisation and Restriction of Chemicals
ESD	Electrostatic Discharge
EPA	ESD Protected Area

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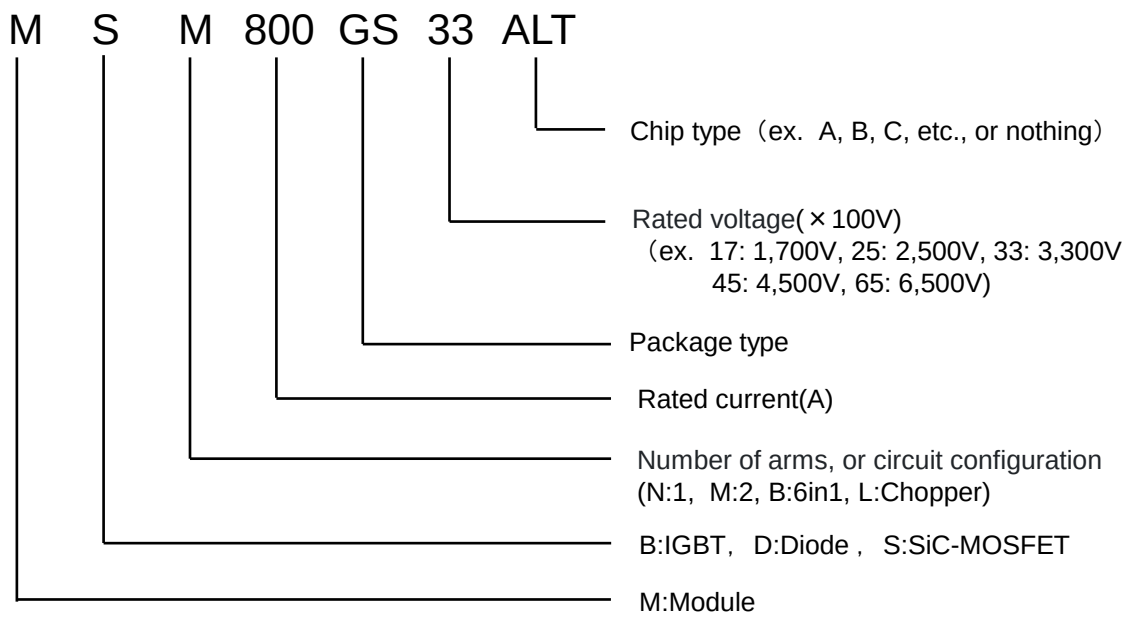
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CHAPTER 1. SiC-MOSFET MODULE

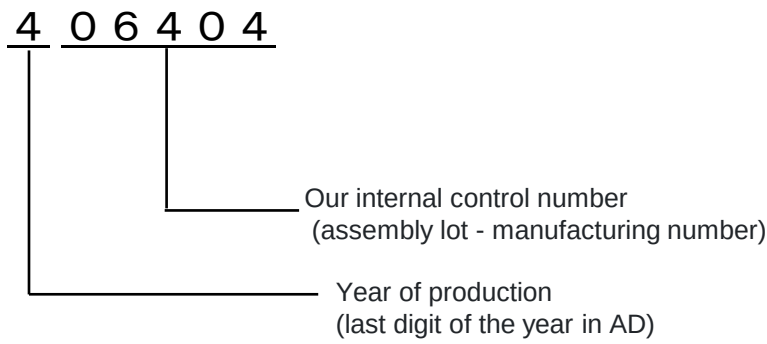
1-1. TYPE DESIGNATION



1-2. MANUFACTURING LOT NUMBER

In addition to the format described above, the nameplate affixed to the product displays the following manufacturing numbers.

Example of a Manufacturing Lot Number :



1-3. BASIC STRUCTURE OF THE MODULE

Figure 1.1 shows a schematic cross-section of the internal structure of the SiC-MOSFET module, especially a single pack module.

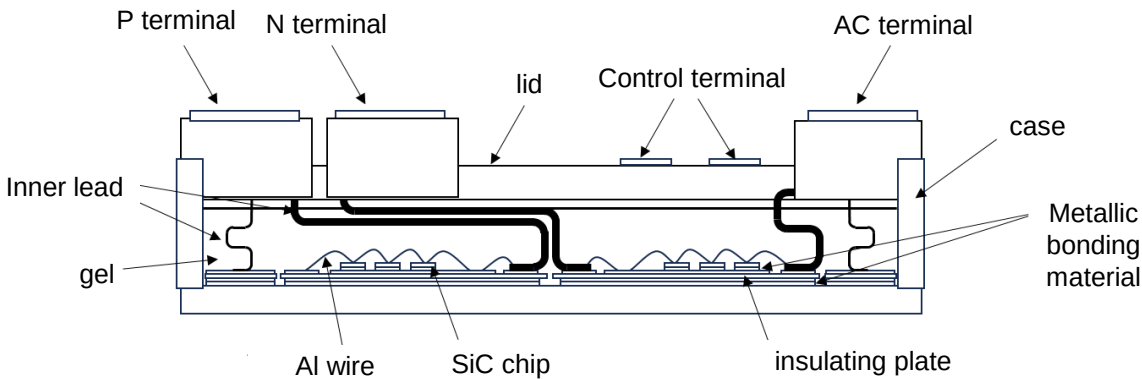


Figure 1.1 Schematic Cross-Section of the SiC-MOSFET Module.

1-4. SiC-MOSFET STRUCTURE

Figure 1.2 shows the cross-sectional structure of a SiC-MOSFET device, illustrating an example of an N-channel vertical planar gate structure. A SiC-MOSFET is a Metal Oxide Semiconductor Field Effect Transistor that utilizes silicon carbide (SiC), a compound semiconductor material composed of silicon (Si) and carbon (C). Since the critical dielectric breakdown field of SiC is approximately 10 times that of Si, the N-SiC epitaxial layer can be made thinner and more heavily doped while maintaining a high breakdown voltage. This enables lower on-resistance $R_{DS(on)}$ compared to conventional Si devices. Furthermore, as a unipolar device, the SiC-MOSFET is capable of faster switching operation compared to Si-IGBTs. Consequently, SiC-MOSFETs are expected to play a key role in power electronics, where the demands for higher power output and voltage continue to grow.

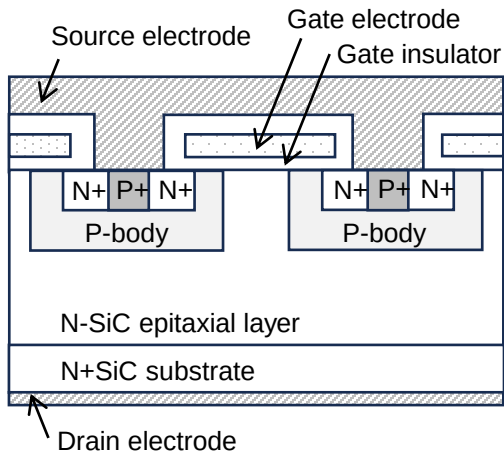


Figure 1.2 Schematic Cross-Section of the SiC-MOSFETs

1-5. SYMBOL AND OPERATING PRINCIPLE OF SiC-MOSFET

1-5-1. Symbol of SiC-MOSFET

Figure 1.3 shows the symbol for an N-channel SiC-MOSFET. In power MOSFETs designed for high-current applications, the body is internally shorted to the source. The device functions as a switch, where conduction between the drain and source is controlled by the gate-source voltage. The parasitic diode formed by the body-source connection is known as the "body diode." As shown in the symbol, this body diode is inherently included in the SiC-MOSFET structure.

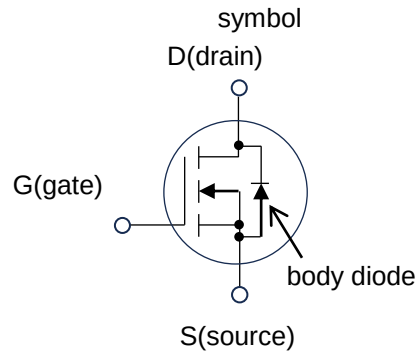


Figure1.3 Symbol of SiC-MOSFET (n-channel)

1-5-2. Operating Principle of the SiC-MOSFET

Figure 1.4 illustrates the operating principle of a SiC-MOSFET. In the planar gate structure (N-channel) shown below, a positive voltage is applied to the drain relative to the source. When a positive gate-source voltage is applied and exceeds the threshold voltage, an inversion layer (channel) is formed in the P-layer beneath the gate insulating film. This transitions the device to the "ON state," allowing drain current to flow from the drain to the source. Conversely, returning the gate voltage to the source potential or applying a negative bias switches the device to the "OFF state," stopping the current flow.

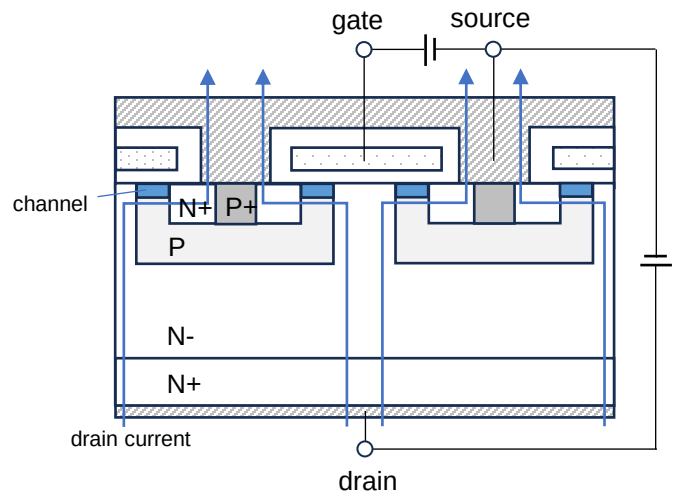


Figure1.4 Operating Principle of the SiC-MOSFET

CHAPTER 2. ITEMS LISTED ON THE SPECIFICATION SHEET



Caution

●When designing electronic circuits using semiconductor devices, ensure that the specified "absolute maximum ratings" of the device are not exceeded under any external condition variations during operation. Additionally, for pulse applications, ensure that the ratings of the "safe operation area (RBSOA · RRSOA)" are not exceeded.

2-1. EXAMPLE OF THE SPECIFICATIONS

An example of the specifications in the following TABLE 2.1

- A) Absolute Maximum Ratings (TABLE 2.1, item ①)
Absolute maximum ratings apply to electrical, mechanical, and thermal conditions that must be adhered to in order to prevent damage to the SiC-MOSFET module. These conditions are generally expressed in terms of maximum or minimum parameter values or as regions of the Safe Operation Area (SOA). (If the module operates outside the listed limits, it may break down.)
- B) Electrical Characteristics (TABLE 2.1, item ②)
This section defines the key electrical characteristics representing the device's function. These parameters are specified under fixed conditions and are expressed as minimum, typical, and maximum values. They are broadly divided into three main categories: static characteristics (DC characteristics), dynamic characteristics (switching characteristics), and thermal characteristics.
- C) Other cautions and notes (TABLE 2.1, items ③ and ④)
Precautions on the maximum rating and other matters are listed.

TABLE 2.1 Specification Example(MSM800GS33ALT)

Minebea Power Semiconductor Device Inc.

SiC MODULE

Spec.No.IGBT-SP-21026 R4 P 1

MSM800GS33ALT

SiC MOSFET 3300V

FEATURES

- Ultra low switching loss with SiC MOSFET
- High current density package
- Low stray inductance & low Rth(j-c)
- Half-bridge (2in1)
- Built in temperature sensor
- Scalable large current easily handled by paralleling
- Equipped with current sensing terminals
- Sintered copper bonding technology
- SBD-less SiC module

Module type

Specification control No.

ABSOLUTE MAXIMUM RATINGS (Tc=25°C)

Item		Symbol	Unit	MSM800GS33ALT
Drain Source Voltage		V _{DS}	V	3,300
Gate Source Voltage		V _{GS}	V	+20/-15
Drain Current	DC	I _D	A	800
	1ms	I _{DM}	A	1,600
Source Current	DC	I _S	A	800
	1ms	I _{SM}	A	1,600
Junction Temperature		T _{vj,op}	°C	-40 ~ +175
Storage Temperature		T _{stg}	°C	-40 ~ +150
Isolation Voltage		V _{ISO}	V _{RMS}	6,000(AC 1 minute)
Screw Torque	Terminals (M3/M8)	M		0.8/15
	Mounting (M8)	M	N·m	8.0 (1)

Notes: (1) Recommended Value 5.5±0.5N·m

①

③

TABLE 2.1 Specification Example(MSM800GS33ALT)

ELECTRICAL CHARACTERISTICS

Item	Symbol	Unit	Min.	Typ.	Max.	Test Conditions
Drain Source Cut-Off Current	I_{OSS}	mA	-	-	0.05	$V_{DS}=3,300V, V_{GS}=0V, T_V=25^{\circ}C$
			-	-	1	$V_{DS}=3,300V, V_{GS}=0V, T_V=175^{\circ}C$
Gate Source Leakage Current	I_{GSS}	nA	-	-	+100	$V_{GS}=20V, V_{DS}=0V, T_V=25^{\circ}C$
			-100	-	-	$V_{GS}=-15V, V_{DS}=0V, T_V=25^{\circ}C$
Drain Source on-state Voltage	$V_{DS(on)}$	V	-	2.3	-	$I_D=800A, V_{GS}=15V, T_V=25^{\circ}C$
			-	4.2	5.5	$I_D=800A, V_{GS}=15V, T_V=175^{\circ}C$
Gate Source Threshold Voltage	$V_{GS(th)}$	V	2.2	3.0	3.8	$V_{DS}=10V, I_D=800mA, T_V=25^{\circ}C$
Input Capacitance	C_{iss}	nF	-	230	-	$V_{DS}=10V, V_{GS}=0V, f=100kHz, T_V=25^{\circ}C$
Internal Gate Resistance	$R_{G(int)}$	Ω	-	2.15	-	
Turn On Delay Time	$t_{d(on)}$		-	1.0	-	$V_{DD}=1,800V, I_D=800A$
Rise Time	t_r	μs	-	0.44	-	$L_S=40nH, R_{G(on/off)}=1/1.5\Omega$ (2)
Turn Off Delay Time	$t_{d(off)}$		-	1.7	-	$V_{GS}=+15/-10V, T_V=175^{\circ}C$
Fall Time	t_f		-	0.25	-	
			-	1.7	-	$I_S=800A, V_{GS}=15V, T_V=25^{\circ}C$
Source Drain Voltage	V_{SD}	V	-	3.8	5	$I_S=800A, V_{GS}=15V, T_V=175^{\circ}C$
			-	8.2	-	$I_S=800A, V_{GS}=10V, T_V=25^{\circ}C$
			-	8.4	-	$I_S=800A, V_{GS}=10V, T_V=175^{\circ}C$
Reverse Recovery Time	t_{rr}	μs	-	0.8	-	$V_{DD}=1,800V, I_S=800A, L_S=40nH, R_{G(on/off)}=1/1.5\Omega, T_V=175^{\circ}C$
Turn On Loss	E_{on}	J/P	-	0.95	-	$V_{DD}=1,800V, I_D=800A, L_S=40nH, R_{G(on/off)}=1/1.5\Omega$ (2)
Turn Off Loss	E_{off}	J/P	-	0.39	-	$V_{GS}=+15V/-10V, T_V=175^{\circ}C$
Reverse Recovery Loss	E_{rr}	J/P	-	0.07	-	
Stray inductance module	L_{SC}	nH	-	10	-	Between D1(main) and S2(main)
	Resistance	R_{DS}	-	5	-	$T_C=25^{\circ}C$
NTC-Thermistor	Deviation	$\Delta R/R$	%	-5	5	$T_C=25^{\circ}C$
	B-constant	$B_{(25/50)}$	K	3375	-	Between $25^{\circ}C$ and $50^{\circ}C$
Thermal Impedance	MOS	$R_{th(j-c)}$	K/W	-	0.024	Junction to case
Contact Thermal Impedance		$R_{th(c-f)}$	K/W	-	0.02	Case to fin(par 1 arm)

Notes: (2) R_G value is a test condition value for evaluation, not recommended value.

Please determine the suitable R_G value by measuring switching behavior and checking results with the respective SOA.

* Please contact our representatives at order.

* For improvement, specifications are subject to change without notice.

* For actual application, please confirm this spec sheet is the newest revision.

* ELECTRICAL CHARACTERISTIC items shown in above table are according to IEC 60747.

2-2. TECHNICAL TERMS

The terms used in specifications and other documents in the following.

TABLE 2.2 Maximum Ratings

Terms		Symbols	Definitions
Drain-Source Voltage		V_{DSS}	Maximum voltage that can be applied between the drain (hereinafter “D”) and source (hereinafter “S”) while the gate (hereinafter “G”) and source are shorted.
Gate-Source Voltage		V_{GSS}	Maximum voltage that can be applied between the gate and source while the drain and source are short-circuited.
Drain Current		I_D	Maximum DC current that can flow continuously from drain to source.
		I_{DM}	Maximum pulsed current that can flow from drain to source with a defined pulse width.
Source Current		I_S	Maximum DC current that can flow continuously from source to drain.
		I_{SM}	Maximum pulsed current that can flow source to drain with a defined pulse width.
Maximum Junction Temperature		T_{vjmax}	Maximum chip temperature at which the device can operate without causing failure.
Operating Junction Temperature		T_{vjop}	Junction temperature at which the device can operate continuously.
Storage Temperature		T_{stg}	Temperature range in which the SiC-MOSFET module can be stored or transported without applying an electrical load.
Isolation Voltage		V_{ISO}	Maximum RMS value of sinusoidal voltage permitted between the terminals and the heat sink mounting surface while all electrodes of the SiC-MOSFET module are short-circuited.
Tightening Torque	Terminals	-	Maximum torque permitted when attaching wiring materials to the terminal section using specified screws or bolts.
	Mounting	-	Maximum torque permitted when connecting the device and external terminals using specified screws or bolts.
	PCB Mounting	-	Maximum torque permitted when attaching a PCB to the device using screws or similar.

2-3. ELECTRICAL CHARACTERISTICS

TABLE 2.3 Static Electrical Characteristics

Term	Symbol	Definition
Drain Source Cut-Off Current	I_{DSS}	Drain leakage current that flows when a specified voltage is applied between D-S while G-S are short-circuited.
Gate Source Leakage Current	I_{GSS}	Gate-source leakage current that flows when a specified voltage is applied between G-S while the G-S are short-circuited.
Gate-Source Threshold Voltage	$V_{GS(th)}$	G-S voltage (in threshold region) at which a specified drain current I_D flows when voltage is applied between G-S, with a specified voltage applied between D-S.
Drain-Source on-state Voltage	$V_{DS(on)}$	D-S voltage when a specified drain current I_D flows at a specified G-S voltage.
Input Capacitance	C_{iss}	Capacitance between G-S, and between D-G, when specified voltages are applied between G-S and D-S while D-S are short-circuited for AC signals.
Output Capacitance	C_{oss}	Sum of the D-S capacitance and D-G capacitance when specified voltages are applied between G-S and D-S while G-S are short-circuited for AC signals.
Reverse transfer Capacitance	C_{rss}	D-G capacitance when specified voltages are applied between G-S and D-S while G-S and D-S are short-circuited for AC signals.
Source-Drain Voltage	V_{SD}	The source-to-drain voltage when a specified source current I_S flows under specified conditions.
Internal Gate Resistance	R_{Gint}	Gate series resistance integrated into the SiC-MOSFET module.
Gate Charge	Q_g	Amount of charge required to be injected into the gate when driving the SiC-MOSFET.
Stray Inductance	L_{SCE}	Stray inductance of the SiC-MOSFET module.

TABLE 2.4 Dynamic Electrical Characteristics

Term	Symbol	Definition
Turn-on Delay Time	$t_{d(on)}$	Time from when the gate voltage reaches 10% of its maximum forward bias value until the drain current reaches 10% of the specified value during the turn-on transition, under the specified conditions.
Rise Time	t_r	Time required for the drain current to rise from 10% to 90% of the specified value.
Turn-off Delay Time	$t_{d(off)}$	Time from when the gate voltage falls to 90% of the maximum forward-bias value until the drain current falls to 90% of the specified value during the turn-off transition, under the specified conditions.
Fall Time	t_f	The time required for the drain current to fall from 90% to 10% of the specified value.
Reverse Recovery Time	t_{rr}	Time required for the reverse recovery current of the SiC-MOSFET body diode to decay to zero, under the specified conditions.
Turn-on Loss	E_{on}	Energy loss generated during the turn-on of the SiC-MOSFET under the specified conditions (see Figure 2.7).
Turn-off Loss	E_{off}	Energy loss generated during the turn-off of the SiC-MOSFET under the specified conditions (see Figure 2.7).
Short Circuit Current	I_{SC}	Maximum current during short circuit.
Short Circuit Withstand Time	t_{SC}	Time from the start of short-circuit current flow until the destruction of the SiC-MOSFET, under the specified circuit conditions.
Reverse Recovery Loss	E_{rr}	Energy loss generated during the reverse recovery of the SiC-MOSFET body diode under the specified conditions (see Figure 2.7).

TABLE 2.5 Thermal Characteristics

Term	Symbol	Definition
Thermal Resistance	$R_{th(j-c)}$	Thermal resistance between the junction of the SiC-MOSFET chip and the case.
	$R_{th(c-f)}$	Thermal resistance between the case and heat sink (fin) when the SiC-MOSFET module is mounted on a heat sink using thermal grease at the recommended torque.
	$R_{th(f-a)}$	Thermal resistance between the heat sink (fin) and the ambient environment.

TABLE 2.6 Thermistor Characteristics

Term	Symbol	Definition
Thermistor Resistance	R	Resistance value between the thermistor terminals under specified temperature conditions.
Thermistor Isolation Current	-	Current that flows between the thermistor terminals and other terminals when a specified voltage is applied, with all terminals other than the thermistor short-circuited.

2-4. CHARACTERISTICS OF SiC-MOSFET MODULE

The following sections describe the typical characteristics, their details, and their intended use, using the 3.3 kV/800 A 2-in-1 SiC-MOSFET module (MSM800GS33ALT) as an example.

2-4-1. Static Characteristics

(1) Drain-Source Voltage vs. Drain Current Characteristics (V_{DS} - I_D Characteristics)

The V_{DS} - I_D characteristics show the relationship between the drain-source voltage V_{DS} and the drain current I_D , using the gate-source voltage V_{GS} as a parameter.

These characteristics are essential for calculating the conduction loss of the SiC-MOSFET.

Figure 2.1(a) and (b) show the V_{DS} - I_D Characteristics at $T_{vj} = 25^{\circ}\text{C}$ and $T_{vj} = 175^{\circ}\text{C}$, respectively.

This device is designed for an on-state operation at $V_{GS} = 15\text{ V}$. Notably, at $V_{GS} < 13\text{ V}$, the drain current I_D tends to increase as the temperature rises, exhibiting a negative temperature coefficient. In parallel-connected configurations, this behavior can lead to current concentration in a specific device, increasing the risk of thermal runaway. Therefore, operating the device in the on-state with $V_{GS} < 13\text{ V}$ is not recommended.

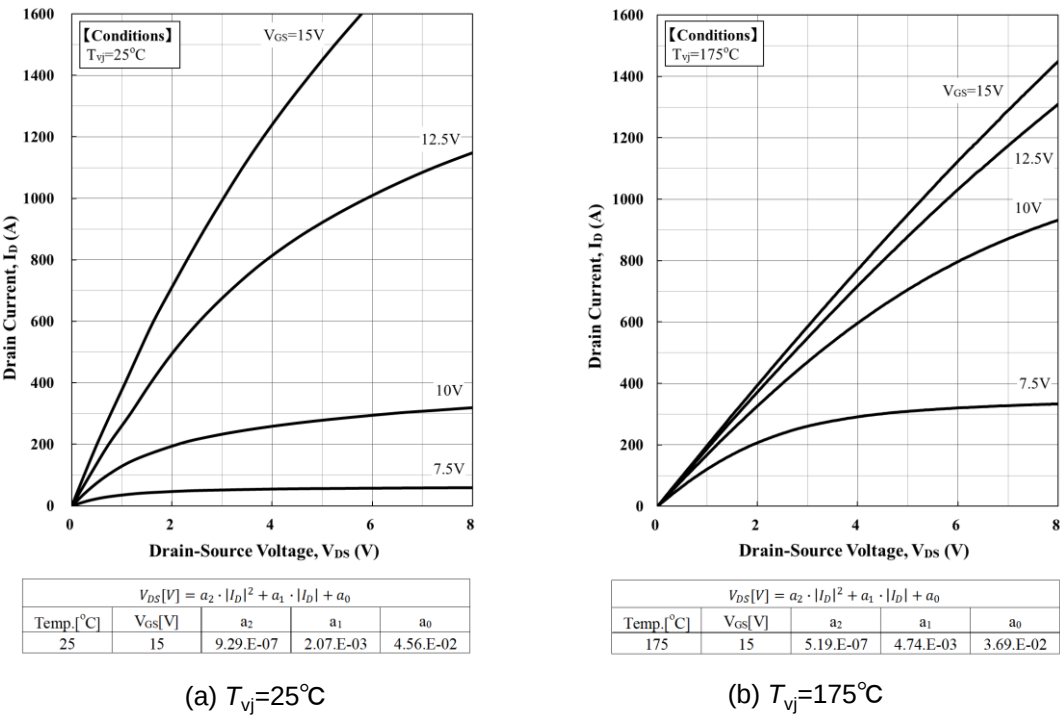


Figure 2.1 Drain Current Vs. Drain-source Voltage Characteristics
(V_{DS} - I_D Characteristics) : Typical

(2) Capacitance Characteristics

Figure 2.2 shows the Gate Charge Characteristics $V_{GS}-Q_g$. These characteristics indicate the total charge required to drive the SiC-MOSFET and are used to determine the necessary power supply capacity for the gate driver circuit. A detailed method for calculating driver circuit losses using these characteristics will be provided in Chapter 3. Additionally, the parasitic capacitances of the SiC-MOSFET are illustrated in Figure 2.3. Figure 2.4 shows the drain-source voltage V_{DS} dependence of the input capacitance C_{iss} , output capacitance C_{oss} , and reverse transfer capacitance C_{rss} . These parameters are essential for gate driver design, including the determination of appropriate dead time.

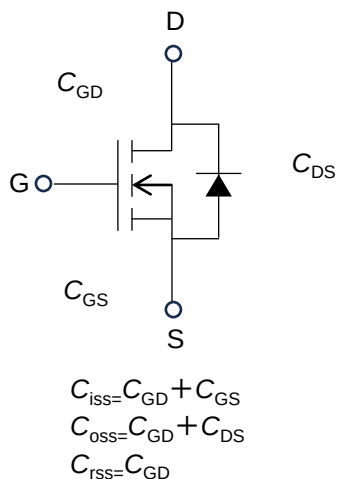


Figure 2.3 Parasitic Characteristics of SiC-MOSFET

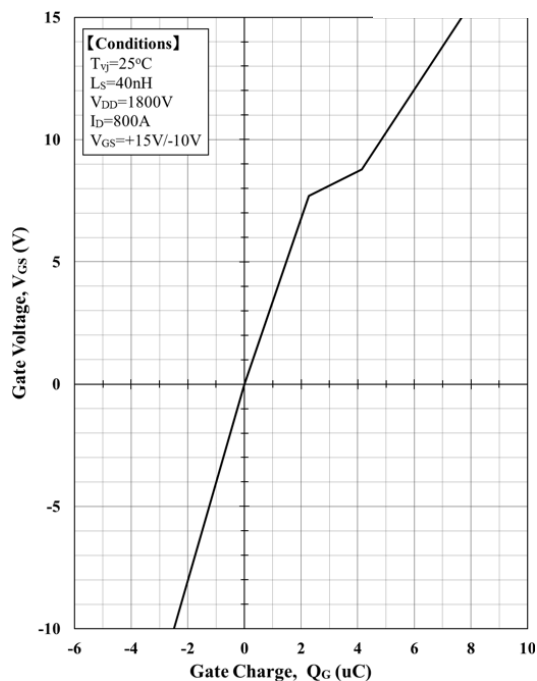


Figure 2.2 Gate Charge Characteristics ($V_{GS}-Q_g$ Characteristics) : Typical

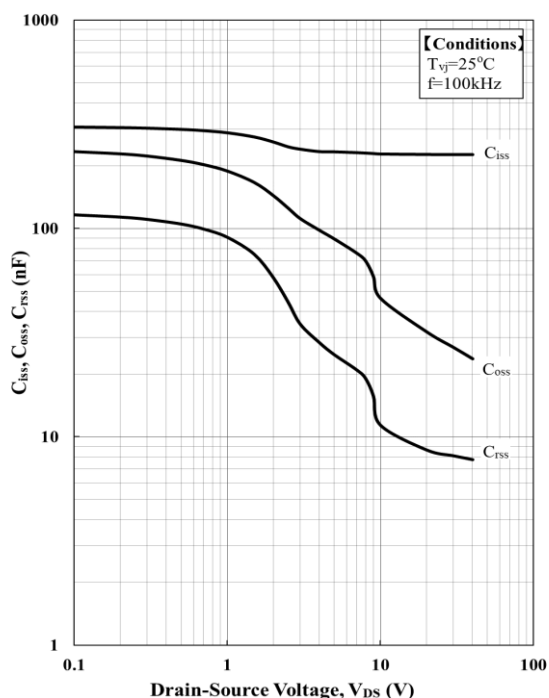


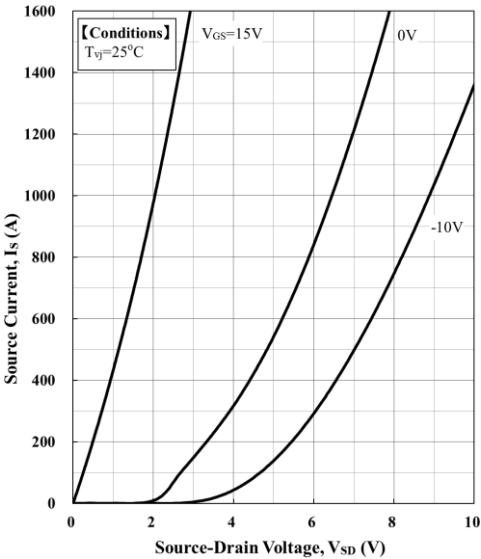
Figure 2.4 Drain-source Voltage Dependency of Parasitic Capacitance : Typical

(3) Source-Drain Voltage vs. Source Current Characteristics (V_{SD} - I_S characteristics)

The V_{SD} - I_S characteristics show the relationship between the source-drain voltage (V_{SD}) and the source current (I_S), using the gate-source voltage (V_{GS}) as a parameter. Figures 2.5(a) and (b) show these characteristics at $T_{vj} = 25\text{ }^{\circ}\text{C}$ and $T_{vj} = 175\text{ }^{\circ}\text{C}$, respectively.

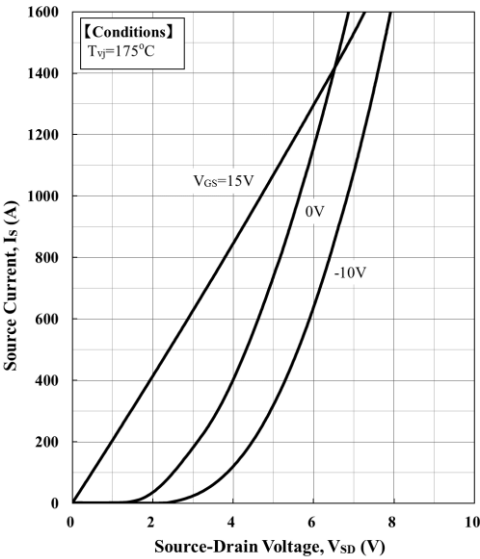
When V_{GS} is negative: In this state, current flows through the internal body diode. These characteristics are used to determine the conduction loss of the body diode. Due to the wide bandgap of SiC, the V_{SD} (forward voltage) is higher than that of standard silicon (Si) devices. Similar to Si, this V_{SD} exhibits a negative temperature coefficient, which must be carefully considered during thermal design.

When V_{GS} is positive: Reverse current can be conducted from the source to the drain through the MOS channel. This mode of operation is known as synchronous rectification and is achieved by applying a standard on-state voltage (e.g., $V_{GS} = +15\text{V}$). As illustrated in Figure 2.5, synchronous rectification significantly reduces conduction losses compared to relying solely on the body diode. Therefore, utilizing this mode is highly recommended. Furthermore, the on-resistance in this mode has a positive temperature coefficient, offering the advantage of automatic current sharing when devices are connected in parallel.



$V_{SD}[\text{V}] = a_2 \cdot I_S ^2 + a_1 \cdot I_S + a_0$				
Temp.[$^{\circ}\text{C}$]	$V_{GS}[\text{V}]$	a_2	a_1	a_0
25	15	-3.70.E-07	2.39.E-03	2.09.E-02

(a) $T_{vj} = 25^{\circ}\text{C}$



$V_{SD}[\text{V}] = a_2 \cdot I_S ^2 + a_1 \cdot I_S + a_0$				
Temp.[$^{\circ}\text{C}$]	$V_{GS}[\text{V}]$	a_2	a_1	a_0
175	15	-2.32.E-07	4.93.E-03	-7.24.E-03

(b) $T_{vj} = 175^{\circ}\text{C}$

Figure 2.5 Source-drain Voltage Vs. Source Current Characteristics
(V_{SD} - I_S Characteristics) : Typical

(4) Temperature Dependence of Maximum Drain-Source Voltage

The drain-source breakdown voltage typically decreases as the junction temperature (T_{vj}). Therefore, when evaluating surge voltages during switching, it is critical to perform verification at the minimum operating temperature. Most devices are designed with a sufficient margin so that the actual breakdown voltage remains above the maximum drain-source voltage (V_{DSS}), even at the minimum T_{vj} .

Consequently, the datasheet often specifies a constant V_{DSS} rating across the entire junction temperature range. However, for certain products, the V_{DSS} rating may be derated at lower temperatures. Please ensure to consult the specific datasheet for each product to confirm its temperature characteristics.

2-4-2. Dynamic Characteristics

The turn-on and turn-off characteristics of a SiC-MOSFET depend on a wide range of parameters, including the drain current (I_D), junction temperature (T_{vj}), gate-source voltage (V_{GS}), and external gate resistance (R_g). Furthermore, since these characteristics are significantly influenced by circuit layout and parasitic inductances, it is strongly recommended to verify switching performance within the actual application environment. Switching characteristics are categorized into two main groups: switching time and switching loss. These can be evaluated using the half-bridge circuit shown in Figure 2.6. Figure 2.7 provides the definitions for the dynamic characteristic parameters listed in TABLE 2.4, such as $t_{d(on)}$, t_r , $t_{d(off)}$, t_f , E_{on} , E_{off} , E_{rr} .

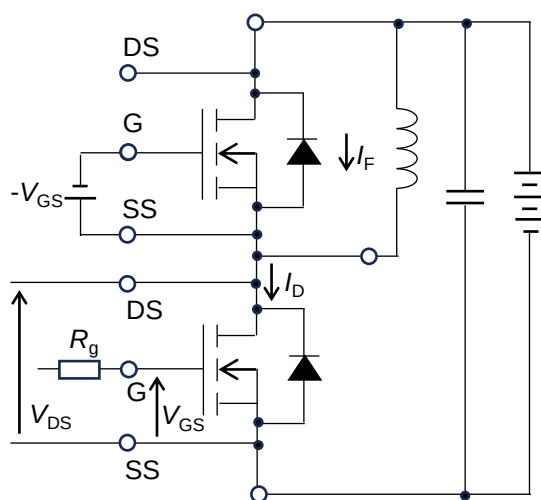


**Figure 2.6 Switching Characteristics Evaluation Circuit
(Half-bridge Circuit)**

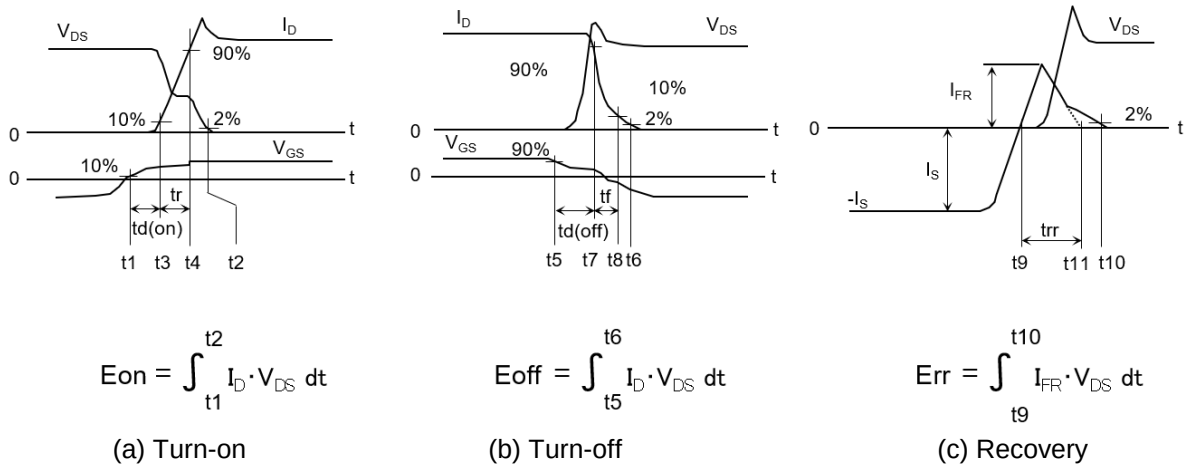


Figure 2.7 Definitions of Switching Characteristics

Figure 2.8 illustrates the drain current (I_D) and source current (I_S) dependence of switching times, while Figure 2.9 shows the gate resistance (R_g) dependence. As indicated, switching times vary significantly with I_D and R_g ; therefore, these factors must be carefully considered during equipment design.

Risks of Prolonged Switching Times: If operating conditions lead to longer switching times, insufficient dead time may result in an upper/lower arm short-circuit (shoot-through). This can cause excessive power loss and potential device destruction.

Risks of Fast Switching (di/dt): Conversely, very short switching times—particularly rapid t_r and t_f —increase the transient current slew rate (di/dt). This induces a surge voltage, calculated as:

$$V_{surge} = L_s \times di/dt$$

where L_s is the circuit's parasitic inductance.

This surge is superimposed on the DC bus voltage and may exceed the RBSOA (Reverse Bias Safe Operating Area), leading to device failure. (Detailed information on RBSOA is provided in Section 2.4.3.)

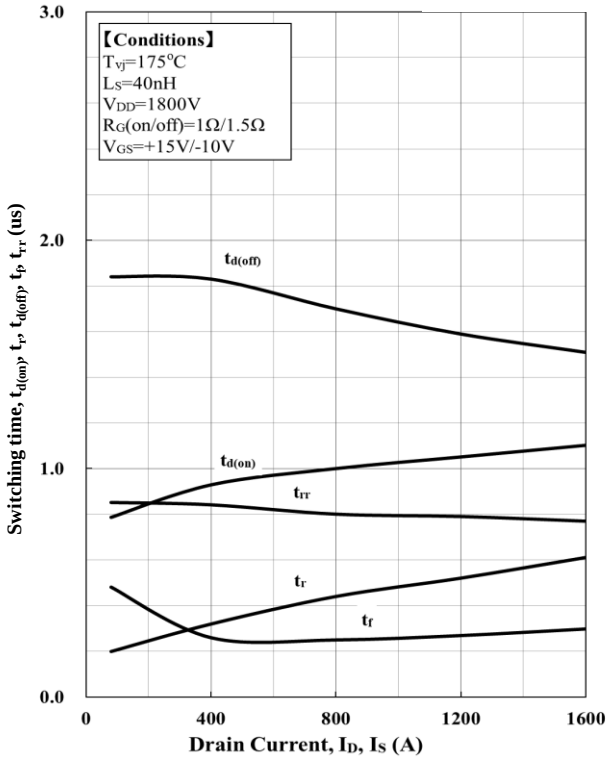


Figure 2.8 I_D, I_S Dependency of Switching Times

: Typical

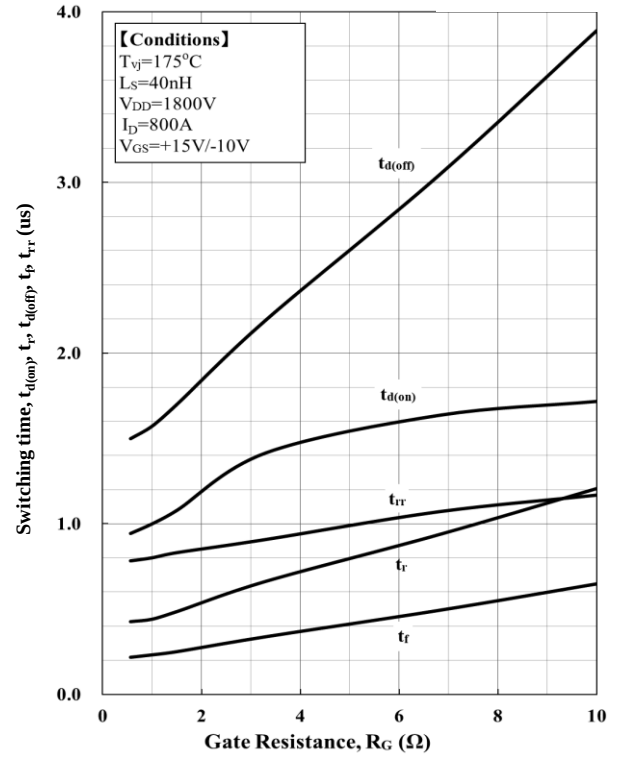


Figure 2.9 R_G Dependency of Switching Times

: Typical

Switching Loss Characteristics E_{on} , E_{off} , E_{rr} : Turn-on loss E_{on} and turn-off loss E_{off} are generated during the SiC-MOSFET's switching transitions, while recovery loss E_{rr} occurs during the reverse recovery of the body diode. For both the MOSFET and the body diode, these losses typically increase at higher junction temperatures T_{vj} .

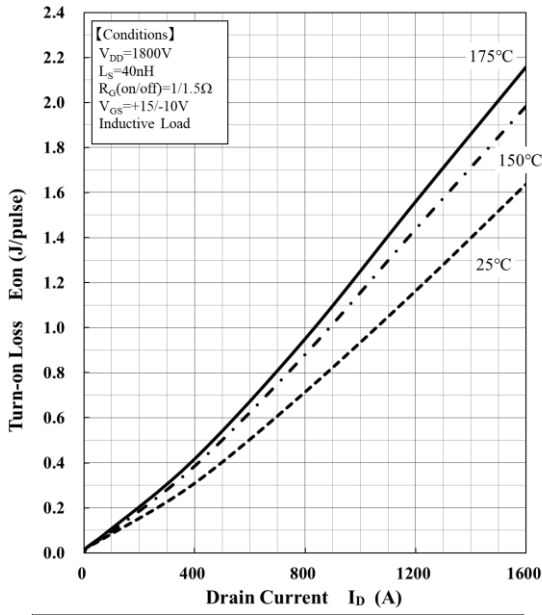
Drain Current I_D Dependence: As shown in Figure 2.10, switching losses increase as I_D rises.

Gate Resistance (R_G) Dependence: Figure 2.11 illustrates the switching loss dependence on the external gate resistance R_G . A smaller R_G reduces switching losses— particularly E_{on} — by shortening the switching times t_r and t_f .

The R_G Selection Trade-off: While a lower R_G improves efficiency, it also results in a higher transient current slew rate di/dt . This increases the surge voltage (V_{surge}) induced by the circuit's total parasitic inductance L_s , calculated as:

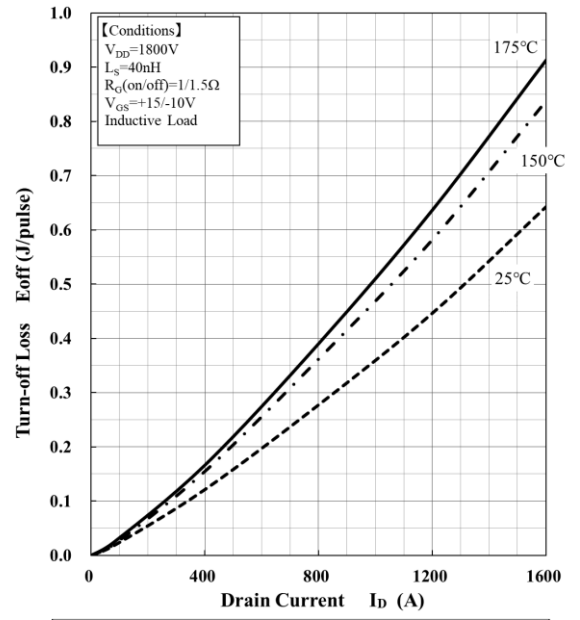
$$V_{surge} = L_s \times di/dt$$

The total parasitic inductance L_s is the sum of the power module's internal inductance and the stray inductance from the DC-link (smoothing) capacitors and the connecting busbars. Therefore, when selecting an optimal R_G value, it is essential to evaluate the switching characteristics using the actual DC-link capacitors, busbars, and gate drive circuitry intended for the final application.



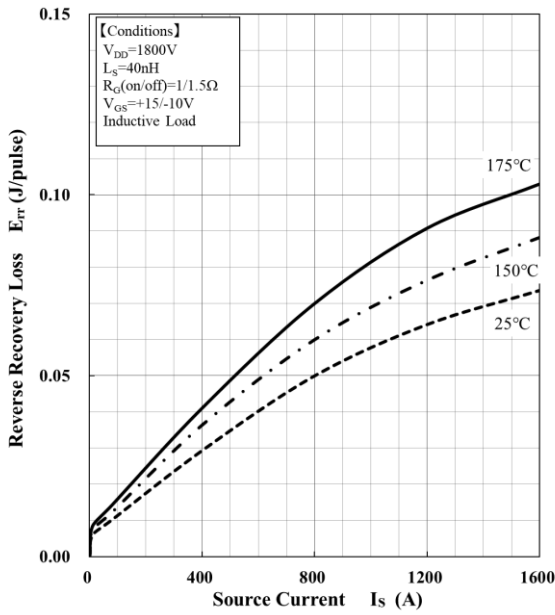
$E [J] = a_2 \cdot I_D ^2 + a_1 \cdot I_D + a_0$			
Temp.[°C]	a ₂	a ₁	a ₀
25	1.78E-07	7.39E-04	5.72E-03
150	1.83E-07	9.56E-04	4.34E-04
175	2.08E-07	1.02.E-03	2.23.E-03

(a) I_D Dependency of Turn-on Loss (E_{on})



$E [J] = a_2 \cdot I_D ^2 + a_1 \cdot I_D + a_0$			
Temp.[°C]	a ₂	a ₁	a ₀
25	7.11E-08	2.90E-04	-3.10E-03
150	9.33E-08	3.78E-04	-5.93E-03
175	1.06E-07	4.05.E-04	-5.64.E-03

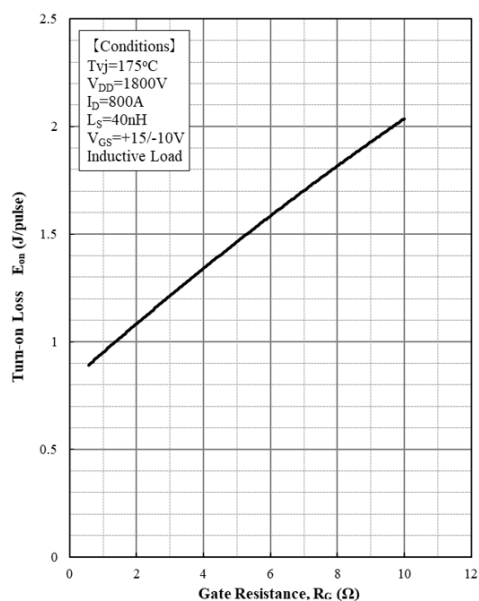
(b) I_D Dependency of Turn-off Loss (E_{off})



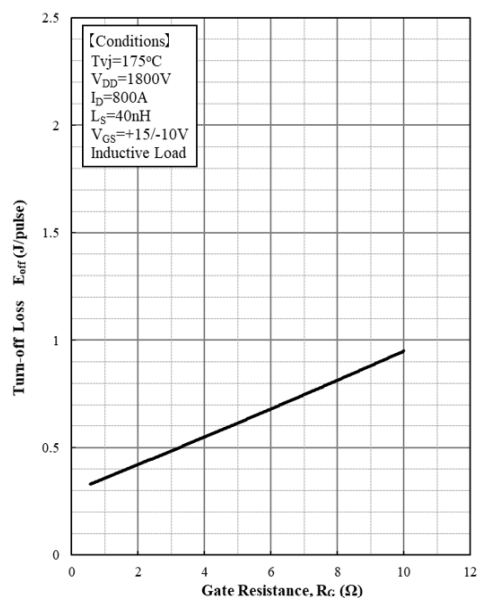
$E [J] = a_2 \cdot I_S ^2 + a_1 \cdot I_S + a_0$			
Temp.[°C]	a ₂	a ₁	a ₀
25	-1.82E-08	7.29E-05	3.22E-03
150	-2.23E-08	8.79E-05	4.07E-03
175	-2.58E-08	1.03.E-04	4.43.E-03

(c) I_S Dependency of Reverse Recovery Loss (E_{rr})

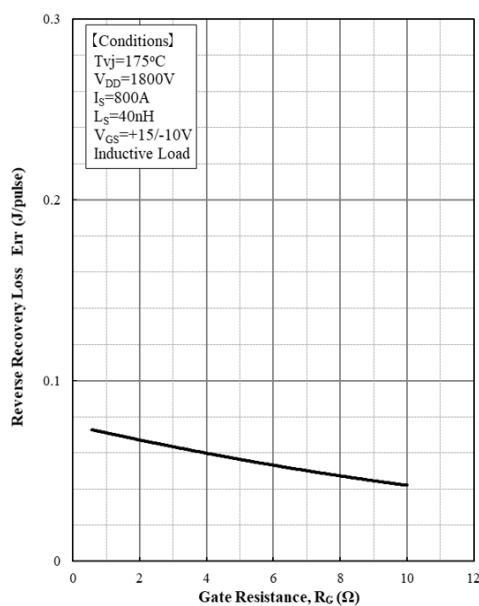
Figure 2.10 I_D , I_S Dependency of Switching Loss : typical



(a) R_g dependency of Turn-on Loss (E_{on})



(b) R_g dependency of Turn-off Loss (E_{off})



(c) R_g dependency of Reverse Recovery Loss (E_{rr})

Figure 2.11 R_g Dependency of Switching Loss : typical

2-4-3. Reverse Bias Safe Operation Area (RBSOA)

The Reverse Bias Safe Operation Area (RBSOA) defines the operating range of drain voltage (V_{DS}) and drain current (I_D) within which the SiC-MOSFET can be safely turned off. Figure 2.12 shows the RBSOA for the MSM800GS33ALT as an example.

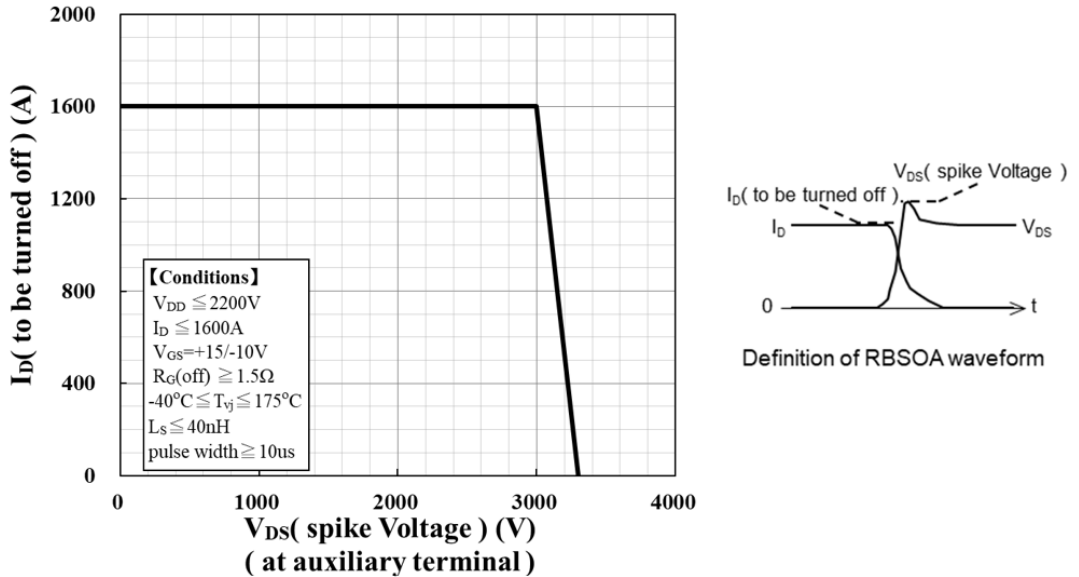


Figure 2.12 Reverse Bias Safe Operation Area (RBSOA)

2-4-4. Reverse Recovery Safe Operation Area (RRSOA)

Similar to the RBSOA of the SiC-MOSFET, a Safe Operating Area (SOA) also exists for the body diode. This is specifically referred to as the Reverse Recovery SOA (RRSOA). It defines the permissible region for the maximum instantaneous power—the product of the current and voltage during the reverse recovery phase. Figure 2.13 illustrates an example of the RRSOA.

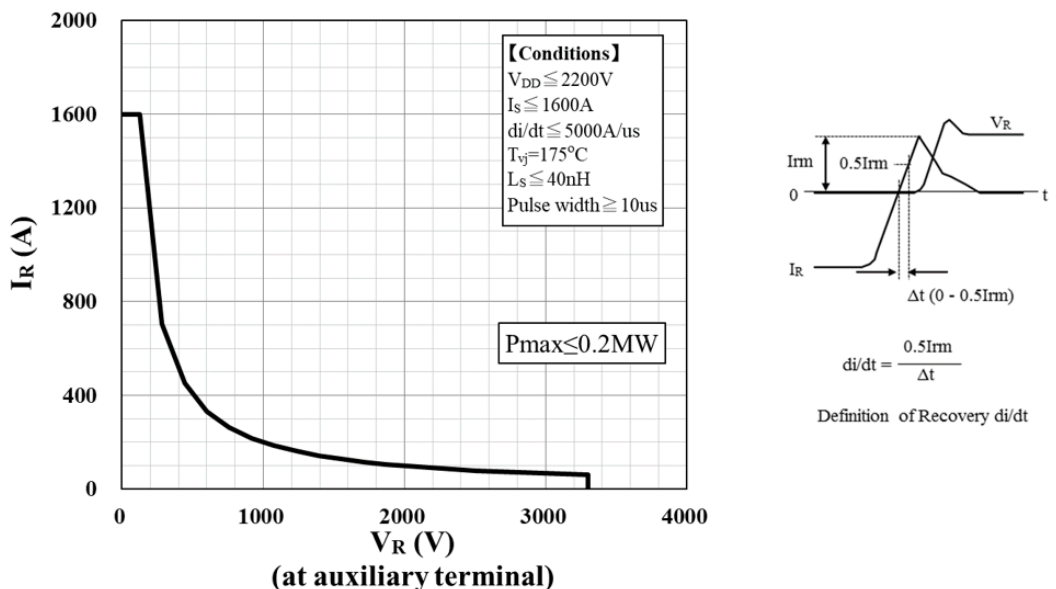


Figure 2.13 Reverse Recovery Safe Operation Area (RRSOA)

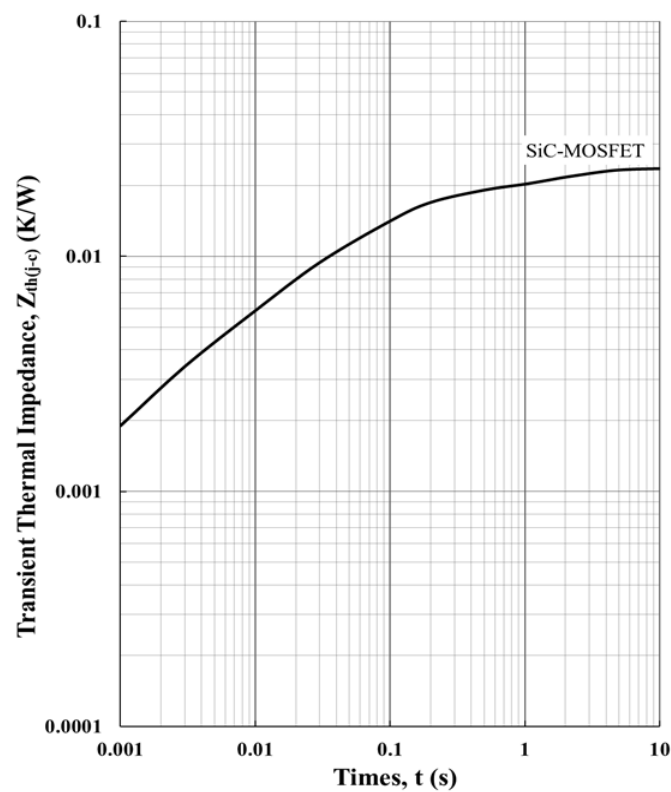
2-4-5. Transient Thermal Impedance

Figure 2.14 shows the transient thermal impedance characteristics, which are used to calculate the temperature rise of the SiC-MOSFET.

Using the transient thermal impedance, the temperature rise is defined by the following equation:

$\Delta T(K) = \text{Thermal Impedance}(K/W) \times \text{Power Loss}(W)$

Details will be described in Chapter 3.



Foster model lumped circuit constant

n	1	2	3	4	Unit
R th, SiC-MOSFET	5.89E-03	1.10E-02	4.70E-03	2.04E-03	K/W
C th, SiC-MOSFET	3.01E+02	8.87E+00	2.46E+00	4.27E-01	J/K

Cauer model lumped circuit constant

n	1	2	3	4	Unit
R th, SiC-MOSFET	3.01E-03	6.75E-03	8.73E-03	5.17E-03	K/W
C th, SiC-MOSFET	3.49E-01	1.82E+00	9.07E+00	3.30E+02	J/K

Transient Thermal Impedance Curve

Figure 2.14 Transient Thermal Impedance

CHAPTER 3. PRECAUTIONS FOR SAFE USE

3-1. DERATING

To ensure device reliability, please apply derating as described below.

While a three-phase inverter is used as an example here, the fundamental principles of derating are applicable to a wide range of other applications.

- Steady-state : 80% or less of the device's rated V_{DSS} (peak voltage)
50% to 60% or less of the device's rated V_{DSS} (DC bus voltage)
- Maximum (transient) : 90% or less of the device's rated V_{DSS} (peak voltage)

In inverter applications, the relationship between the device's voltage rating and the power supply voltage (input AC line voltage) can be estimated using the following equation:

$$V_{DSS} = V_{in} \times \sqrt{2} + V_{surge} + V_{reg} + \alpha \quad \text{---(1)}$$

V_{DSS} ; Device rated voltage

V_{in} ; Input voltage (AC RMS voltage)

V_{surge} ; Surge voltage (spike)

V_{reg} ; Increase in DC bus voltage (e.g., due to regeneration)

α ; Design margin / safety factor

(1) Current

- Steady-state : 50% to 60% or less of the device's rated DC current (repetitive peak current)
- Maximum (transient) : 90% or less of the device's rated DC current (repetitive peak current)

However, if derating is already implemented based on the junction temperature (T_{vj}), the current derating is inherently accounted for by this thermal limit. Please note that the 1 ms surge current rating (I_{SM}) specified in the datasheet is intended for non-repetitive events, such as peak currents during body diode reverse recovery or transient fault conditions (e.g., load short-circuit protection).

The device must not be operated repetitively in a manner that induces thermal cycling from such peak events, as this can degrade long-term reliability. The required DC drain current rating, considering the necessary derating, can be estimated as follows:

$$I_p = P_{inv} \times \kappa \div V_{ac} \div \sqrt{3} \times \sqrt{2} \times \lambda \quad \text{---(2)}$$

$$I_D > I_p \div \beta \quad \text{---(3)}$$

I_p ; Peak current

P_{inv} ; Inverter capacity

κ ; Overload factor

V_{ac} ; AC voltage (RMS)

λ ; Current ripple rate

I_D ; Rated DC current of the device (Rated drain current)

β ; Derating factor

(3) Junction Temperature

- Steady-state : 80% or less of the maximum rated junction temperature
- Maximum (transient) : 90% or less of the maximum rated junction temperature
- The case temperature (T_C) should be kept at 100 °C or below during operation.

Please be aware that thermal cycling (repeated changes in the junction temperature (T_{vj}) and case temperature (T_C)) induces stress on the module's internal components, which will cause a reduction in module lifetime.

For details, please refer to Section 3-5, "Thermal Resistance and Thermal Design".

3-2. GATE DRIVER CIRCUIT

The voltage and current waveforms of a SiC-MOSFET during switching are significantly influenced by the forward gate bias ($+V_{GS}$), reverse gate bias ($-V_{GS}$), and gate resistance (R_g). Therefore, these parameters must be optimized to meet the specific design targets of the application.

Precautions for configuring $+V_{GS}$, $-V_{GS}$, and R_g are detailed below.

3.2.1. Forward Gate Bias: $+V_{GS}$;

Maximum Rating: The $+V_{GS}$ must be designed to strictly remain below the maximum gate-source voltage rating of 20 V.

(2) Voltage Tolerance: It is recommended to maintain gate power supply voltage fluctuations within $\pm 10\%$.

(3) Conduction Loss: During the on-state, a higher $+V_{GS}$ reduces the on-state voltage drop ($V_{DS(on)}$) and on-resistance ($R_{DS(on)}$). This results in reduced steady-state conduction loss.

(4) Turn-on Loss vs. Surge: While a higher $+V_{GS}$ decreases turn-on loss (E_{on}), it also increases the recovery dv/dt and di/dt of the opposing arm's diode (freewheeling diode). This leads to a higher surge voltage during diode recovery.

(5) Turn-off Loss: Turn-off loss (E_{off}) is relatively insensitive to gate voltage variations, provided the fluctuation remains within $\pm 10\%$.

(6) Short-Circuit Capability: A higher V_{GS} increases the saturation current, which leads to a higher short-circuit current. Consequently, the short-circuit withstand capability is reduced.

3-2-2. Reverse Gate Bias : $-V_{GS}$

- (1) Maximum Rating: Ensure that $|-V_{GS}|$ does not exceed the maximum gate-source voltage rating. Since the maximum rating and recommended voltage vary by product, please refer to the respective product datasheet.
- (2) Voltage Tolerance: It is recommended to maintain the fluctuation of the gate power supply voltage within $\pm 10\%$.
- (3) Turn-off Speed vs. Surge: A larger absolute value of $-V_{GS}$ (more negative bias) shortens the turn-off time and reduces turn-off loss (E_{off}). However, this also results in a higher surge voltage.
- (4) False Turn-on Risk: dV/dt -induced false turn-on (parasitic turn-on) is more likely to occur with a small absolute value of $-V_{GS}$ (insufficient reverse bias).

3-2-3. Gate Resistance : R_g

The gate resistance (R_g) value listed in the datasheet's "Testing conditions" section are the turn-on and turn-off R_g values that were selected in our test environment. These values were used to measure the switching times and losses using the recommended gate voltage, while operating within the absolute maximum ratings.

- (1) Regarding switching times: As R_g increases, the turn-on and turn-off delay times ($t_{d(on)}$, $t_{d(off)}$, etc.,) tend to become longer.
- (2) Regarding switching losses: Turn-on loss (E_{on}) and turn-off loss (E_{off}) increase as R_g increases. Conversely, recovery loss (E_{rr}) decreases as R_g increases.
- (3) All switching characteristics change significantly depending on the parasitic inductance of the circuit layout. In particular, the surge voltage generated during SiC-MOSFET turn-off and diode recovery is heavily affected. Therefore, please design your R_g value after minimizing the circuit's parasitic inductance as much as possible.

3-2-4. Avoiding dV/dt Induced False Turn-on During Recovery

Figure 3.1 illustrates the mechanism of false turn-on (parasitic turn-on) caused by high dV_{DS}/dt during reverse recovery. Assume a condition where the low-side SiC-MOSFET (SiC-MOSFET2) is OFF, and a freewheeling current ① (I_F) flows through the body diode (D1) of the high-side SiC-MOSFET (SiC-MOSFET1). When SiC-MOSFET2 transitions to the ON state from this condition, a drain current ② (I_D) begins to flow. At this moment, D1 enters reverse recovery. Consequently, the drain-source voltage ③ (V_{DS}) of SiC-MOSFET1 rises sharply, generating a high dV_{DS}/dt . This rapid voltage change induces a displacement current, $I_G = C_{rss} \times dV_{DS}/dt$, which flows into the gate of SiC-MOSFET1 through its reverse transfer capacitance (C_{rss} , or Miller capacitance). As this current flows through the gate resistance (R_g), it lifts the gate voltage (V_{GS}) of SiC-MOSFET1 in the positive direction.

If this induced voltage spike exceeds the sum of the applied reverse bias ($-V_{GS}$) and the device's threshold voltage (V_{th}), SiC-MOSFET1 will falsely turn on. This results in both SiC-MOSFET1 and SiC-MOSFET2 being on simultaneously, causing a shoot-through (arm short-circuit) condition.

To prevent this false turn-on, the following countermeasures can be implemented:

- Increase the negative reverse bias voltage ($-V_{GS}$): Provides a larger safety margin against voltage spikes.
- Increase the gate resistance (R_g): Slows down the switching speed of the opposing switch to reduce the dV_{DS}/dt .
- Add an external gate-source capacitor (C_{GS}): Absorbs the induced charge and suppresses the voltage rise.
- Active Miller Clamping: Actively shorts the gate and source terminals during the off-state.

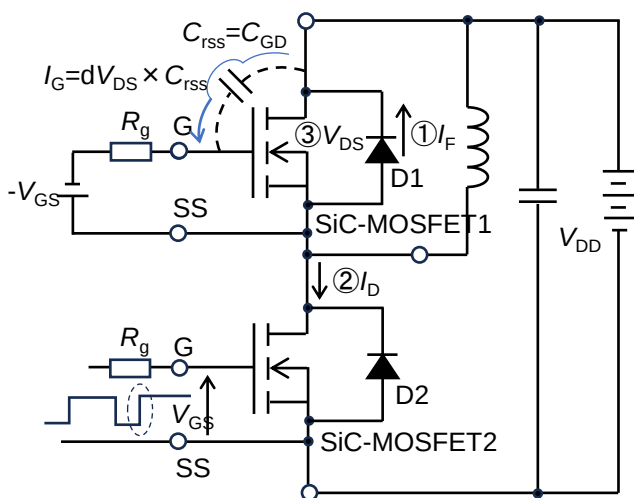
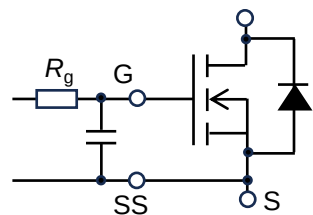
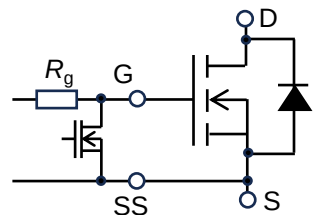


Figure 3.1 Principle of False Turn-on Caused by dV_{DS}/dt During Recovery



(c) Insert a capacitor between Gate and Source



(d) Short the Gate and Source terminals during the off-state

Figure 3.2 False Turn-on Prevention Methods

However, it is important to consider the trade-offs associated with these methods:

- (a) May lead to an increased turn-off surge voltage.
- (b) Causes higher turn-on switching losses.
- (c) Increases the load on the gate driver (higher driver losses).
- (d) Complicates the gate driver circuit design.

3-2-5. Gate Driver Power

SiC-MOSFETs are turned on and off by charging and discharging the gate capacitance. The peak gate current (I_{Gp}) can be approximated by the following equation:

$$I_{Gp} = \frac{|+V_{GS}| + |-V_{GS}|}{R_g + r_g} \quad \text{---(4)}$$

$+V_{GS}$: Forward gate bias

$-V_{GS}$: Reverse gate bias

R_g : External gate resistance

r_g : Internal gate resistance

Using the Gate Charge Characteristics (V_{GS} - Q_g) shown in Figure 3.3, the average gate current (I_G) and the gate drive power required to drive the SiC-MOSFET can be calculated.

$$I_G = f_c \times (|+Q_g| + |-Q_g|) \quad \text{---(5)}$$

f_c : Carrier frequency

$+Q_g$: Total charge from 0V to $+V_{GS}$

$-Q_g$: Total charge from 0V to $-V_{GS}$

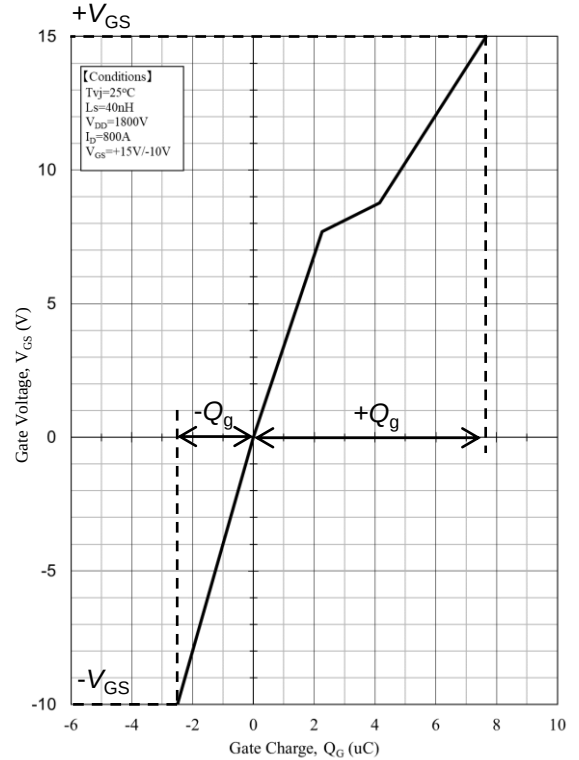


Figure 3.3 Gate Charge Characteristics
(V_{GS} - Q_g) : Typical

Additionally, the power for turn-on $P_{d(on)}$ and the power for turn-off $P_{d(off)}$ are given by:

$$P_{d(on)} = P_{d(off)} = f_c \times \{1/2 \times (|Q_g| + |-Q_g|) \times (|+V_G| + |-V_G|)\} \quad \text{---(6)}$$

From this, the total gate driver power (P_d) is:

$$P_d = f_c \times \{(|Q_g| + |-Q_g|) \times (|+V_G| + |-V_G|)\} \quad \text{---(7)}$$

Please design the driver circuit so that it is capable of supplying the drive current and drive power as described above.

Also, please select a gate resistor (R_g) with a power rating sufficient to tolerate the generated power loss calculated by Equation (7).

3-2-6. Synchronous Rectification Mode and Dead Time

As referenced in TABLE 2.1 of Chapter 2, this application note uses the MSM800GS33ALT as a specification example. This SiC-MOSFET contains an intrinsic body diode. Due to the wide bandgap properties of Silicon Carbide (SiC), the forward voltage of this body diode (V_{SD} at $V_{GS} = 0V$ to $-10V$) is significantly higher than that of silicon (Si) devices. Synchronous rectification is an operating mode used to mitigate this high forward voltage and reduce conduction losses. For applications utilizing only the SiC-MOSFET (i.e., without a parallel SiC-SBD), this mode is highly recommended. It works by applying a positive gate voltage (e.g., $+15V$) to allow reverse current to flow through the channel rather than the diode. (This state corresponds to a lower V_{SD} at $V_{GS} = +15V$)

Figure 3.4 illustrates an example of synchronous rectification and dead time. Dead time must be inserted to prevent the high-side and low-side SiC-MOSFETs from turning on simultaneously (shoot-through). During this dead time, the freewheeling current flows through the body diode. As noted earlier, since the body diode's forward voltage is high, the dead time duration should be minimized to reduce conduction losses. However, the minimum required dead time depends on factors such as the SiC-MOSFET switching speed and gate driver propagation delays. Therefore, careful consideration of these factors is necessary when determining the final dead time setting. Further details on dead time design will be discussed in the following pages.

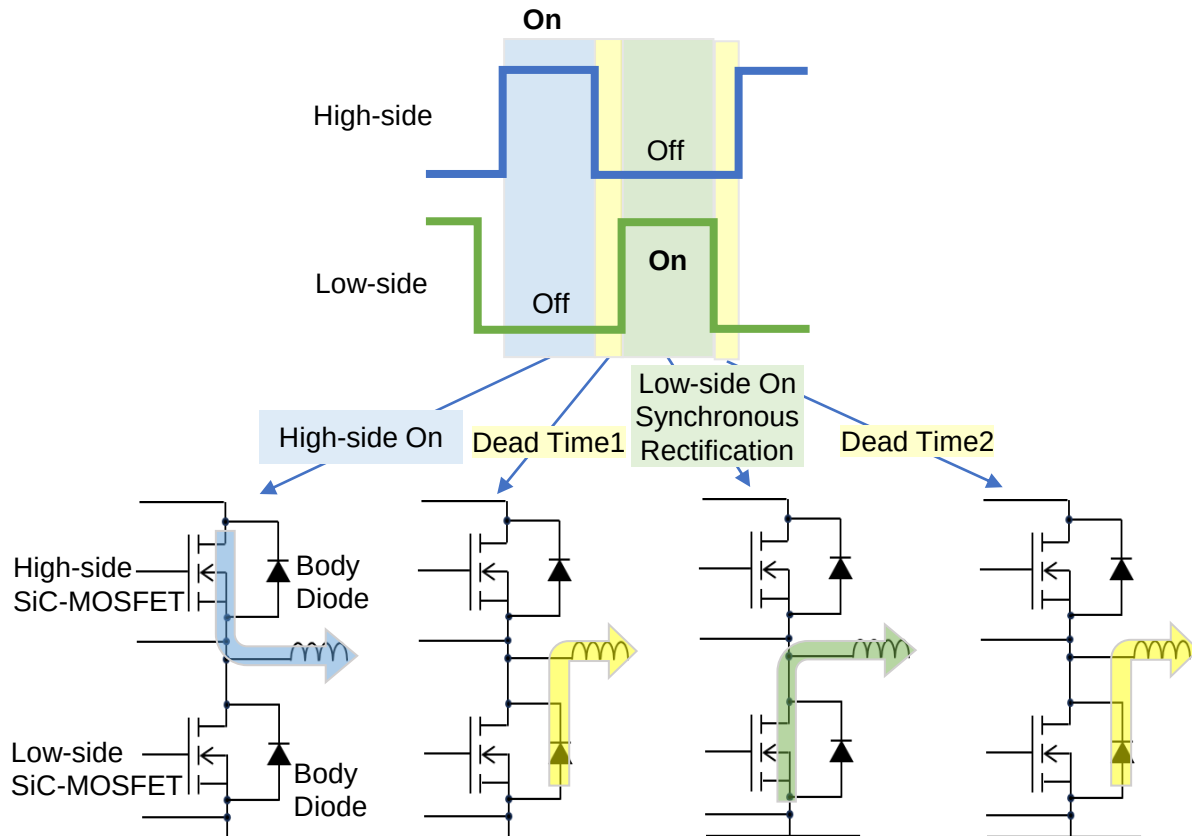


Figure 3.4 An Example of Synchronous Rectification Mode and Dead Time

3-2-7. Dead Time

This section details the principles of dead time and its relation to SiC-MOSFET operation. If the high-side and low-side arms turn on simultaneously, it causes an arm short-circuit (shoot-through), resulting in excessive current flow that can damage the devices. Therefore, it is critical to configure an appropriate dead time and implement overcurrent protection. The relationship between the dead time defined in the control logic and the actual dead time observed at the SiC-MOSFET is explained below.

(1) Main Circuit Configuration Example

Figure 3.5 illustrates a circuit configuration for one phase leg of a voltage-source inverter. In this example, a high-side and a low-side arm are connected across the DC link terminals (P and N) of a DC voltage source, E_o . This setup assumes an operating mode where the high-side and low-side SiC-MOSFETs switch complementarily (alternately turning on and off). To prevent short-circuits caused by simultaneous conduction, an off-period—known as dead time or non-overlap time—is inserted into the control signals ensuring both SiC-MOSFETs remain off during transitions.

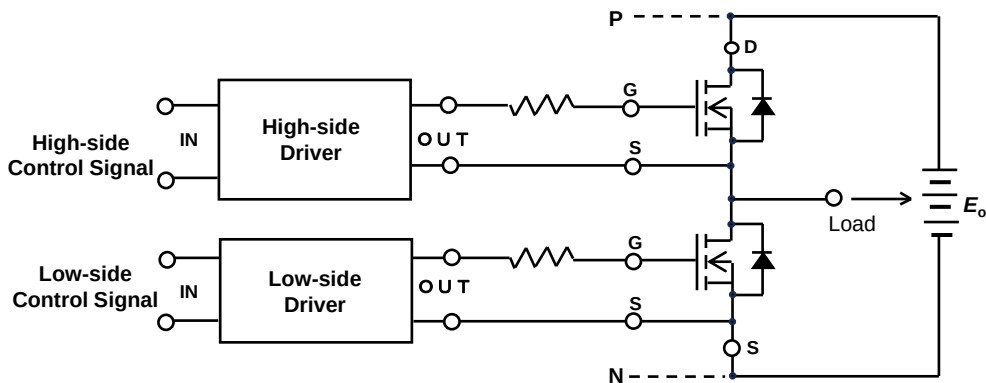


**Figure 3.5 Main Circuit Configuration Example
(Single-Phase Arm Configuration)**

(2) Dead Time in Logic vs. Dead Time at the SiC-MOSFET Output Terminals (D, S)

Figure 3.6 illustrates the timing relationship between the control signals, the gate driver output voltage, and the SiC-MOSFET drain-source voltage (V_{DS}). The dead time configured in the logic circuit (denoted as T_D) results in an effective dead time (T_{D_e}) at the device level.

This discrepancy is caused by the following propagation delays:

- Gate driver propagation delays (t_1 and t_3 in Figure 3.6)
- SiC-MOSFET switching delays (t_2 and t_4 in Figure 3.6)

The respective delay times, t_1 to t_4 , are defined as follows:

- t_1 : Turn-on control signal input $\rightarrow$ Driver output voltage rise (Turn-on delay)
- t_2 : Driver output voltage rise $\rightarrow$ SiC-MOSFET turn-on (Device switching delay)
- t_3 : Turn-off control signal input $\rightarrow$ Driver output voltage fall (Turn-off delay)
- t_4 : Driver output voltage fall $\rightarrow$ SiC-MOSFET turn-off (Device switching delay)

(Note: This analysis assumes that the delay characteristics are symmetrical between the high-side and low-side arms.)

The relationship between the dead time set in the logic (T_D) and the actual dead time at the SiC-MOSFET's D-S terminals (T_D') is given by the following equation:

$$T_D' = T_D - (t_3 + t_4) + (t_1 + t_2) \quad \text{---(8)}$$

As indicated by the equation, the dead time configured in the logic (T_D) is altered by the cumulative delay times (t_1 through t_4), resulting in the effective dead time (T_D'). Therefore, it is essential to accurately analyze and verify the propagation delays within the gate driver circuit (t_1 , t_3) as well as the switching delays of the SiC-MOSFET (t_2 , t_4).

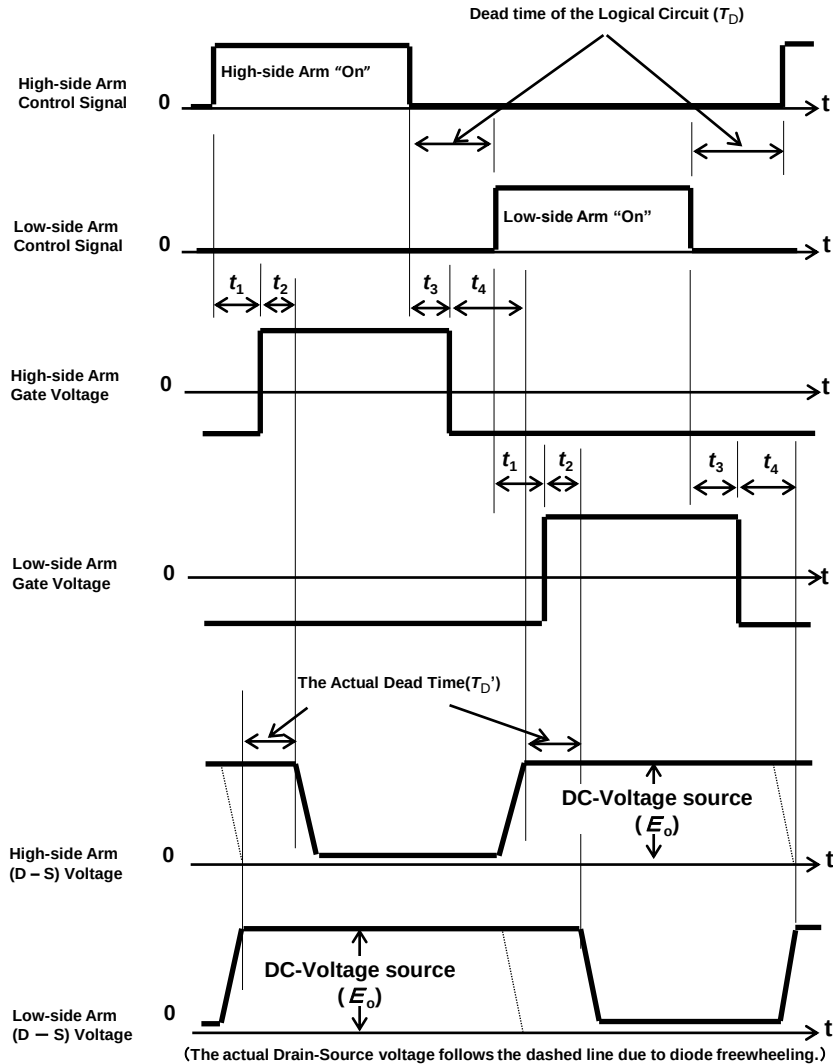


Figure 3.6 the Relationship Between Control Signal, Gate Voltage, and SiC-MOSFET D-S Voltage

3-3. PARALLEL CONNECTION

3-3-1. Relationship Between On-state Voltage Variation ($\Delta V_{DS(on)}$) and Current Imbalance Rate

When operating SiC-MOSFETs in parallel, current imbalances may arise due to mismatches in wiring inductance (resulting from the physical circuit layout), variations in the gate drive circuit, or differences in driving conditions. Therefore, a thorough system evaluation is essential prior to implementation. Please contact us for further details.

The current imbalance ratio (α) for a two-device parallel connection is defined as follows:

$$\alpha = \left(\frac{I_D'}{(I_{total} \div 2)} - 1 \right) \times 100(\%) \quad \text{---(9)}$$

I_D' : Current of one device

I_{total} : Total current for two device in parallel

This definition is typically applied at the rated current. However, it is important to note that even with identical devices, the current imbalance ratio (α) can vary significantly depending on the total current level.

Regarding series connections, ensuring uniform voltage sharing is challenging. There is a risk that the voltage applied to a specific device may exceed its breakdown voltage. Therefore, in addition to matching static characteristics such as on-state voltage ($V_{DS(on)}$), it is essential to match dynamic characteristics like turn-on delay ($t_{d(on)}$) and turn-off delay ($t_{d(off)}$). Furthermore, external voltage-balancing circuitry, such as voltage-balancing resistors or snubber circuits, is required to equalize the voltage across the series-connected devices.

3-3-2. Number of Parallel Devices and Current Derating Factor

Theoretically, there is no upper limit to the number of devices that can be connected in parallel. However, practical limitations arise due to the physical size of the layout and the associated increase in parasitic inductance, which can lead to higher surge voltages.

Let n denote the number of parallel devices. Assuming a worst-case scenario where current concentrates on a single device, the current derating factor (R) can be calculated using the equation below. Here, α represents the current imbalance ratio defined earlier.

$$R = \frac{1 + (n-1) \times (1 - \frac{\alpha}{100}) \div (1 + \frac{\alpha}{100})}{n} \times 100(\%) \quad \text{---(10)}$$

Calculation Example : When using for 600 A devices in parallel ($n=4$), if we assume an imbalance rate $\alpha = 15\%$, then $R = 80.4\%$. Therefore, the total allowable current in this case is:

$$600A \times 4_{\text{parallel}} \times 0.804 = 1,929 \text{ (A)}$$

3-3-3. Fundamental Guidelines for Parallel Connection

In general, the following three key factors must be addressed to ensure stable parallel operation:

(a) Steady-State Balance: To minimize steady-state current imbalance, select devices with matched on-state voltage ($V_{DS(on)}$) characteristics (i.e., narrow parameter distribution).

(b) Transient Balance: To minimize transient current imbalance during turn-on and turn-off, ensure symmetrical wiring in both the gate drive circuit and the main power loop to eliminate inductance mismatches.

(c) Thermal Balance: Ensure uniform cooling conditions for all parallel-connected modules to prevent temperature discrepancies between them.

Figure 3.7 illustrates an implementation example of a 3-phase, 2-parallel configuration utilizing the nHPD2 package and its associated busbars. In this design, the layout is optimized to minimize the inductance of the DC and AC connections while ensuring symmetry.

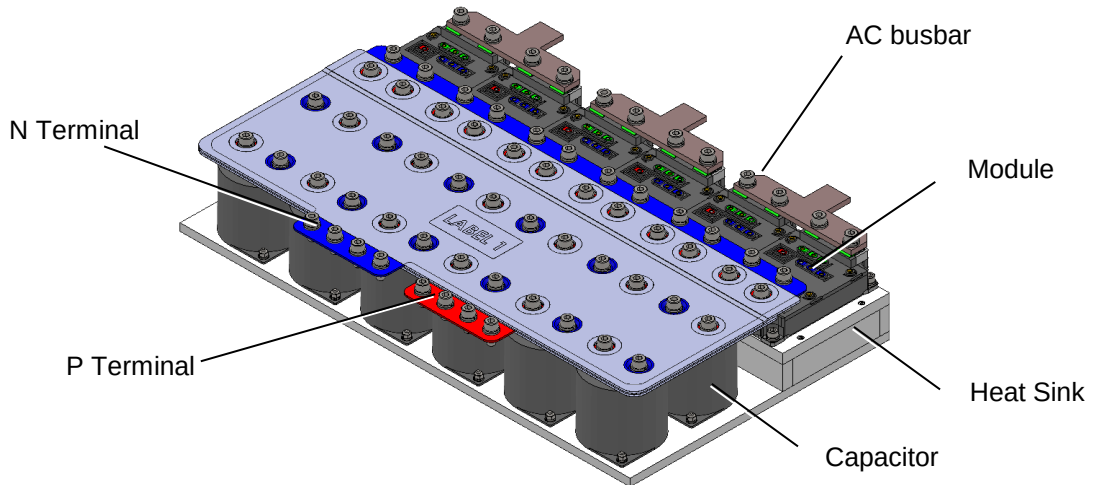


Figure 3.7 An implementation example of a 3-phase, 2-parallel configuration using the nHPD2

(1) Single Driver Configuration per Arm

When driving parallel-connected devices, a single gate driver unit (including isolation stages such as optocouplers, amplifiers, and overcurrent protection) must be used for each arm, regardless of the number of parallel SiC-MOSFETs. This is strictly required to prevent parallel operation issues caused by propagation delay skew between individual drivers.

(2) Gate Resistor Configuration for Parallel Devices

To suppress gate voltage oscillations during switching, connect the driver to the parallel devices as shown in Figure 3.8, ensuring that each module is equipped with its own individual gate resistor.

Please adhere to the following wiring guidelines regarding Figure 3.8:

- (a) Low Impedance Wiring: Use twisted-pair cables for the driver output wiring to minimize impedance.
- (b) Symmetrical Layout: Ensure that the loop inductances (L_{gst}) in loops A and B are identical and minimized as much as possible. (Note: Both (a) and (b) are critical measures to prevent malfunctions caused by inductive noise during main circuit switching.)
- (c) Oscillation Damping: Gate voltage oscillations can occur during both turn-on and turn-off. Oscillation after turn-off is particularly critical, as it can induce false turn-on, leading to failures such as arm short-circuit (shoot-through). To prevent this, ensure that the relationship between the gate resistance (R_g) and the loop inductance (L_{gst}) satisfies Equation (11).
(Here, C_{iss} represents the input capacitance of the SiC-MOSFET.)

$$2 \times R_g > 2 \sqrt{\frac{L_{gst} \times 2}{C_{iss}/2}} \quad \text{---(11)}$$

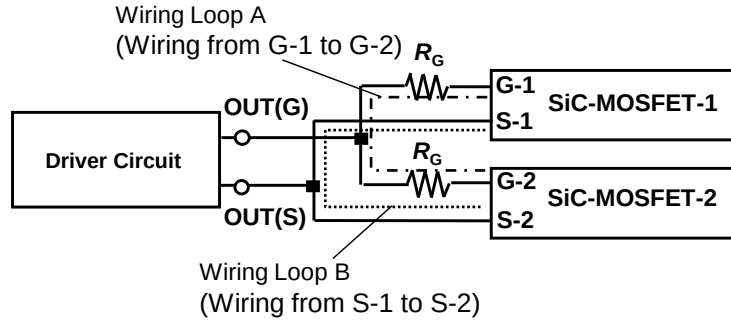


Figure 3.8 Connection Example of Parallel-Connected Modules and a Driver Circuit

3-3-4. Necessity of Symmetrical Main Circuit Wiring

(1) Balancing Main Circuit Inductance

For parallel-connected SiC-MOSFETs, the drain-side and source-side wiring must be designed symmetrically to ensure that their respective parasitic inductances are balanced.

Figure 3.9 illustrates the equivalent circuit for a two-device parallel configuration, explicitly showing the parasitic inductances of the main power loop. In this diagram, the variables are defined as follows:

- L_{DA} : Drain-side wiring inductance of SiC-MOSFET(A)
- L_{DB} : Drain-side wiring inductance of SiC-MOSFET(B)
- L_{SA} : Source-side wiring inductance of SiC-MOSFET(A)
- L_{SB} : Source-side wiring inductance of SiC-MOSFET(B)

During the turn-on transition of SiC-MOSFETs (A) and (B), the current distribution is significantly affected by variations in these wiring inductances. It is important to note that transient current sharing is determined almost entirely by the ratio of these inductances. Therefore, ensuring wiring symmetry (i.e., matching the inductance values) is essential for safe operation.

Figure 3.10 illustrates the current sharing characteristics under an imbalanced scenario (referencing Figure 3.9). In this case, the total wiring inductance of device A is lower than that of device B ($L_{DA} + L_{SA} < L_{DB} + L_{SB}$), and the on-state voltage ($V_{DS(on)}$) of SiC-MOSFET (A) is lower than that of SiC-MOSFET (B). Particular attention must be paid to any imbalance in the source-side wiring (L_{SA} , L_{SB}). Mismatches in source inductance are critical because they directly modulate the effective gate-source voltage, significantly exacerbating the current imbalance.

This phenomenon occurs because the rapid change in current during switching generates an induced voltage ($V = L \times di/dt$) across the source inductances (L_{SA} and L_{SB}). If these inductances differ, the resulting induced voltages will create a differential bias between the gate-source terminals of the parallel SiC-MOSFETs, causing one device to switch faster than the other.

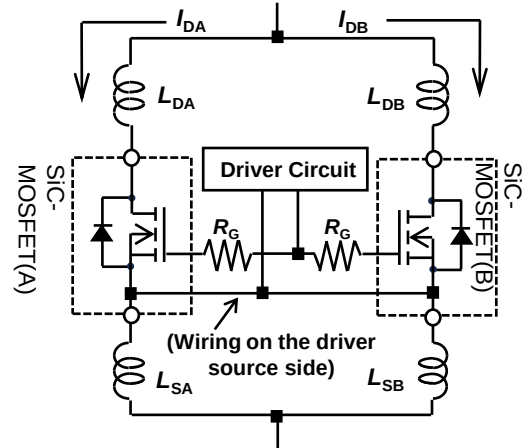


Figure 3.9 Main Wiring Inductance in Parallel Connection

A symmetrical wiring layout is required to equalize L_{DA} and L_{DB} , and L_{SA} and L_{SB} , respectively.

(2) Duration of Transient Current Imbalance due to Main Circuit

As showed in Figure 3.10, the transient current imbalance observed during turn-on gradually stabilizes during the SiC-MOSFET's steady on-state. The currents converge towards their respective steady-state values (I_{DA} and I_{DB}), which are determined by the on-state voltage ($V_{DS(on)}$) characteristics. The time required for this stabilization can be modeled as the transient response of an R-L circuit. This equivalent circuit consists of the total inductance within the closed loop of the parallel configuration and the on-state resistance of the SiC-MOSFET devices. The device on-state resistance (r_{on}) can be derived from the output characteristic curve. For example, in the case of the MSM800GS33ALT, r_{on} is approximately $2.9\text{m}\Omega$ (at $T_{vj} = 25^\circ\text{C}$ and half the rated current). Assuming the total loop inductance ($L_{DA} + L_{DB} + L_{SA} + L_{SB}$) is 40 nH , the current equalization process is governed by the time constant τ , as defined by Equation (12) below.

$$\tau = \frac{40\text{nH}}{2.9\text{m}\Omega \times 2} = 6.9\mu\text{s} \quad \text{---(12)}$$

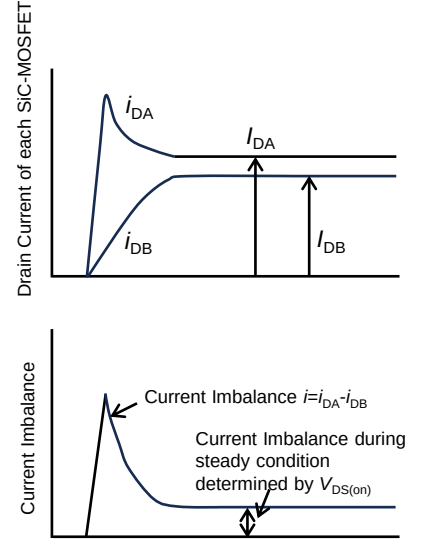


Figure 3.10 Current Imbalance Equalization

3-4. THERMAL DESIGN METHOD

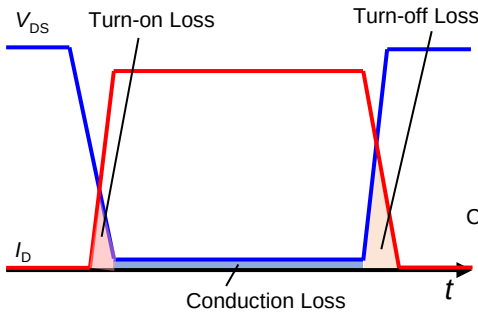
3-4-1. Power Loss Composition of SiC-MOSFET Modules

The SiC-MOSFET module comprises the SiC-MOSFET device and its intrinsic body diode.

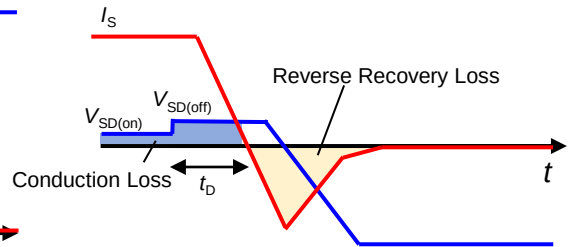
Consequently, the total power loss of the module is calculated as the sum of the losses generated by both components. These losses are classified into two primary categories :

- Conduction Loss: Occurs during the steady on-state.
- Switching Loss: Occurs during the transient switching transitions (turn-on and turn-off).

Figure 3.11 Shows the Schematic Switching Waveforms for Both the SiC-MOSFET and the Body diode, along with their associated power loss components.



(a) Power Loss of SiC-MOSFET



(b) Power Loss of the Body Diode

Figure 3.11 Schematic Switching Waveforms and Power Losses for the SiC-MOSFET and Body Diode

$$\text{Module Loss}(P_{\text{total}}) = (\text{Number of arms}) \times \{\text{SiC-MOSFET Loss}(P_{\text{mos}}) + \text{Diode Loss}(P_{\text{diode}})\} \quad \text{--- (13)}$$

$$P_{\text{mos}} = \text{Conduction Loss}(P_{\text{on}}) + \text{Turn-on Loss}(P_{\text{ton}}) + \text{Turn-off Loss}(P_{\text{toff}}) \quad \text{--- (14)}$$

$$P_{\text{diode}} = \text{Forward Conduction Loss}(P_f) + \text{Reverse Recovery Loss}(P_{rr}) \quad \text{--- (15)}$$

3-4-2. Loss Calculation

This section introduces a simplified method for calculating losses when a SiC-MOSFET is used in a PWM-controlled inverter circuit. The calculation is based on the following assumptions:

- (a) The PWM control is for a three-phase 2-level inverter.
- (b) The PWM method is sinusoidal modulation based on a triangular wave comparison.
- (c) The output current is an ideal sine wave.

Figure 3.12 shows the schematic operation waveforms of the 2-level inverter based on the assumptions above.

(1) Conduction loss

If the RMS value of the inverter's output phase current is I_o , the sinusoidal output current I_D is expressed by the equation below.

$$I_D = \sqrt{2} \times I_o \times \sin \theta \quad \text{--- (16)}$$

Letting m be the modulation index and $\cos \phi$ be the lagging power factor of the current, the SiC-MOSFET on-duty waveform $D(\theta)$ is:

$$D = \frac{1+m \times \sin(\theta+\phi)}{2} \quad \text{--- (17)}$$

When the drain current I_D flows through the SiC-MOSFET, $V_{\text{DS(on)}}$ is generated across the drain and source. The relationship between $V_{\text{DS(on)}}$ and I_D is described in the datasheet. If the relationship between $V_{\text{DS(on)}}$ and I_D is linearly approximated as shown in Fig.3.13,

$$V_{\text{DS(on)}} = I_D \times r_{\text{DS(on)}} \quad \text{--- (18)}$$

From Equations (17) and (18), the SiC-MOSFET conduction loss P_{on} per arm in the inverter circuit is given by:

$$\begin{aligned} P_{\text{on}} &= \frac{1}{2\pi} \int_0^\pi I_D \times V_{\text{DS(on)}} \times D \, d\theta \\ &= \frac{I_o^2 r_{\text{DS(on)}} (8m \cos \phi + 3\pi)}{12\pi} \quad \text{--- (19)} \end{aligned}$$

Where, I_D : Drain current flowing through the SiC-MOSFET (instantaneous value)

$V_{\text{DS(on)}}$: Drain-source on-voltage of the SiC-MOSFET (instantaneous value)

The conduction loss during reverse conduction must be calculated separately for two conditions —when the SiC-MOSFET is off (during the dead-time) and when it is on— and then these results must be added together. When the SiC-MOSFET is off, the reverse conduction current flows through the body diode. The V_{SD}/I_S relationship for this condition is linearly approximated as shown in Figure 3.13.

$$V_{\text{SD(off)}} = V_{f0} + I_S \times r_{\text{SD(off)}} \quad \text{--- (20)}$$

Where the reverse conduction current I_S is expressed by the following equation:

$$I_S = -\sqrt{2} \times I_0 \times \sin \theta \quad \text{---(21)}$$

Furthermore, when the SiC-MOSFET is on, the reverse conduction flows through the MOS channel. The V_{SD} - I_S relationship for this condition is linearly approximated as shown in Figure 3.13.

$$V_{SD(on)} = I_S \times r_{SD(on)} \quad \text{---(22)}$$

In this case, the conduction loss P_f generated by the reverse conduction current is expressed by the following equation:

$$P_f = \frac{1}{2\pi} \int_{\pi}^{2\pi} (I_S \times V_{SD(on)} \times (D - t_D \times f_{sw}) + I_S \times V_{SD(off)} \times 2t_D \times f_{sw}) d\theta$$

$$= \frac{I_0^2 \cdot (12\pi f_{sw} r_{SD(off)} t_D - 6\pi f_{sw} r_{SD(on)} t_D - 8\pi r_{SD(on)} \cos \phi + 3\pi r_{SD(on)}) + 24\sqrt{2} I_0 V_{fo} f_{sw} t_D}{12\pi} \quad \text{---(23)}$$

Where, I_S : Source current flowing through the SiC-MOSFET (instantaneous value),
 $V_{SD(off)}$: Source-drain off-state voltage of the SiC-MOSFET (instantaneous value),
 $V_{SD(on)}$: Source-drain on-state voltage of the SiC-MOSFET (instantaneous value),
 t_D : Dead-time

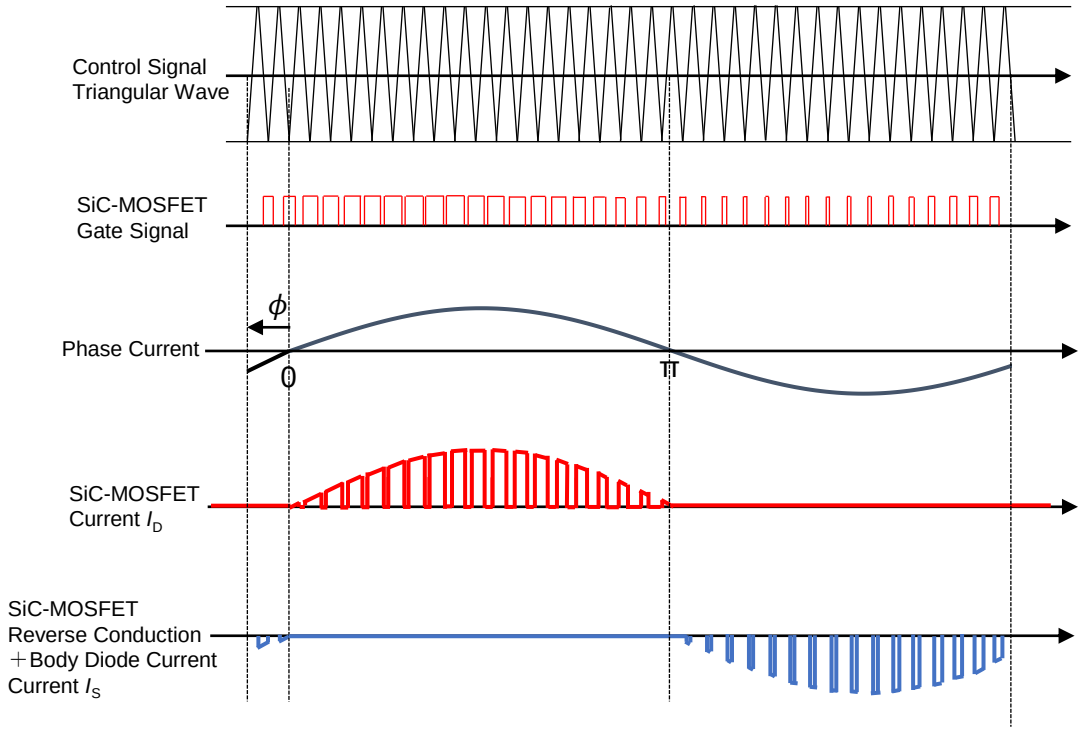
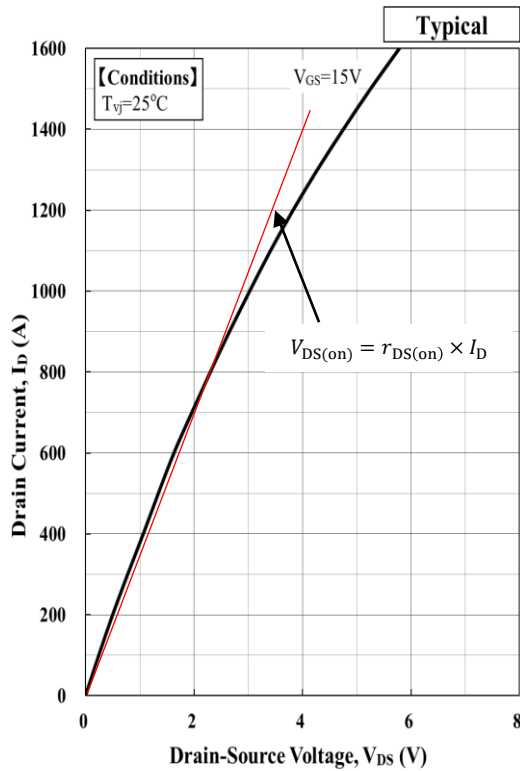
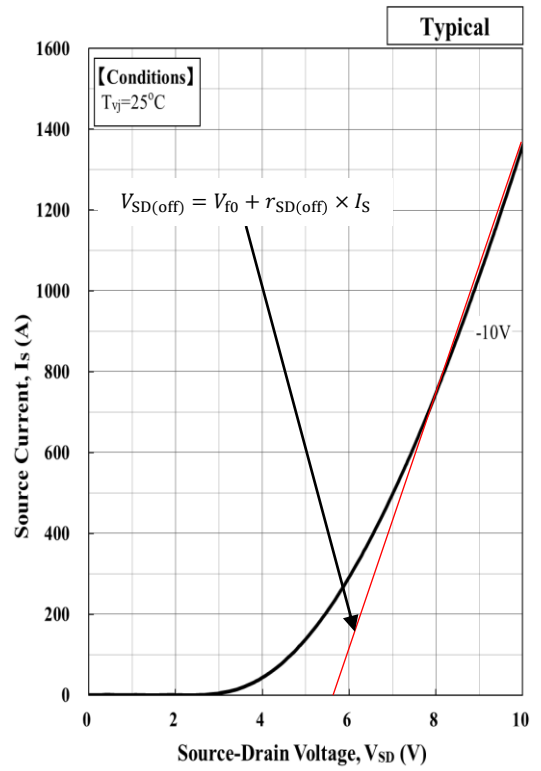


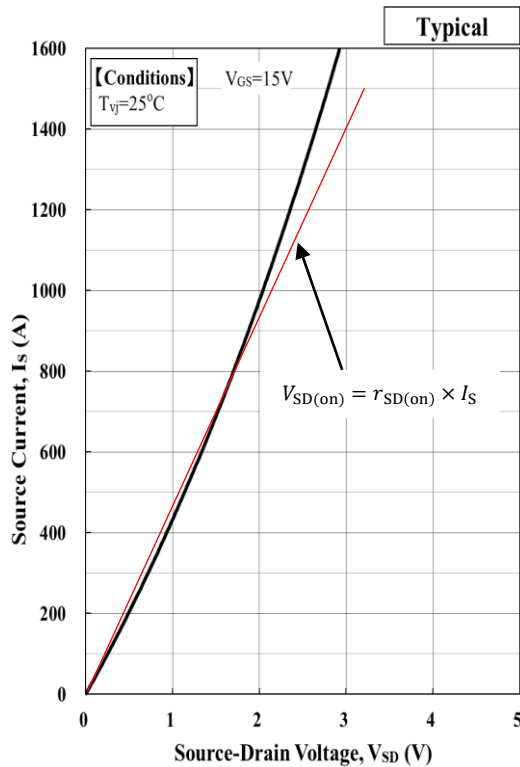
Figure 3.12 Schematic Operation Waveforms of a 2-level Inverter



(a) SiC-MOSFET ($V_{GS} = 15\text{V}$)



(b) Body Diode ($V_{GS} = -10\text{V}$)



(c) MOSFET Reverse Conduction
+ Body Diode ($V_{GS} = 15\text{V}$)

Figure 3.13 Linear Approximation of SiC-MOSFET and Diode Output Characteristics

Switching Loss

This section explains the method for calculating switching loss from the I_D dependency of E_{on} , E_{off} , and E_{rr} , which is described in the datasheet. If the I_D dependency of E_{on} is linearly approximated, that is,

$$E_{on}(I_D) = k_{on} \times I_D \quad \text{---(24)}$$

$$\begin{aligned} P_{ton} &= \frac{1}{2\pi} \int_0^\pi E_{on}(I_D) \times f_{sw} d\theta \\ &= \frac{1}{2\pi} \int_0^\pi k_{on} \times \sqrt{2} \times I_0 \times \sin\theta \times f_{sw} d\theta \\ &= \frac{\sqrt{2}}{\pi} \times k_{on} \times I_0 \times f_{sw} \quad \text{---(25)} \end{aligned}$$

Where, f_{sw} : Carrier frequency

Now, the average output current I_{ave} is:

$$I_{ave} = \frac{2}{\pi} \times \sqrt{2} \times I_0 \quad \text{---(26)}$$

If E_{on} at I_{ave} is defined as E_{ton} , then using Equation (26), Equation (25) becomes:

$$P_{ton} = E_{ton} \times \frac{f_{sw}}{2} \quad \text{---(27)}$$

Similarly,

$$P_{toff} = E_{toff} \times \frac{f_{sw}}{2} \quad \text{---(28)}$$

$$P_{rr} = E_{rr} \times \frac{f_{sw}}{2} \quad \text{---(29)}$$

3-5. THERMAL RESISTANCE AND THERMAL DESIGN

3-5-1. Thermal Resistance

Regarding the module's thermal resistance, the junction-to-case thermal resistance, $R_{th(j-c)}$, for the SiC-MOSFET device is specified in the datasheet.

3-5-2. Definition of Temperature Measurement Points

The definition of the measurement locations for the case temperature and heat sink temperature is shown in Figure 3.14. The junction-to case thermal resistance, and the case-to-heat sink contact thermal resistance, $R_{th(c-f)}$, are specified in accordance with this definition.

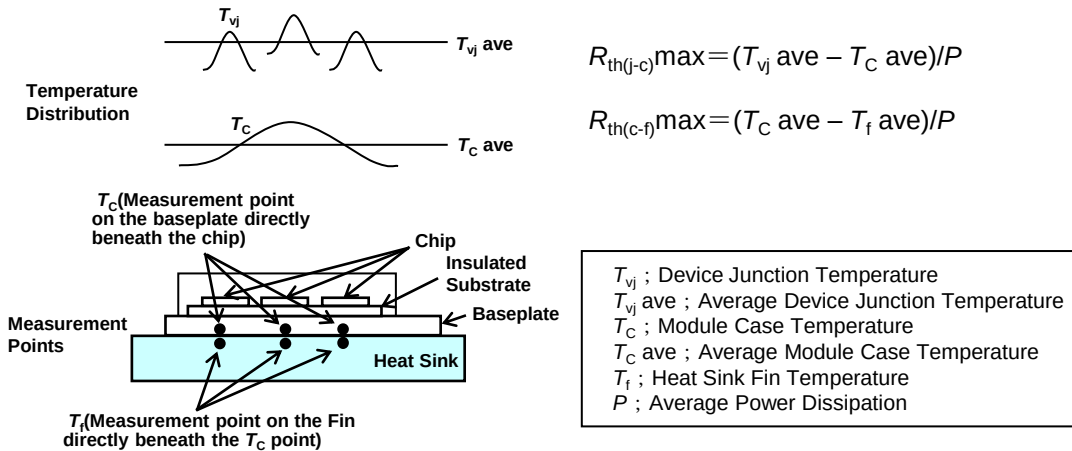


Figure 3.14 Temperature Measurement Points

3-5-3. Thermal Design Considerations

The following section describes the fundamental concepts of steady-state and transient conditions essential for heat sink selection.

(1) Steady State

Figure 3.15 shows the thermal equivalent circuit under steady-state conditions.

Based on the thermal equivalent circuit in Figure 3.15, the junction temperature of the SiC-MOSFET, $T_{vj}(\text{SiC-MOSFET})$, can be calculated using the following equation:

$$\begin{aligned} T_{vj}(\text{SiC-MOSFET}) = & \{P(\text{SiC-MOSFET}) + P(\text{Body Diode})\} \times R_{th(j-c)}(\text{SiC-MOSFET}) \\ & + \{P(\text{SiC-MOSFET}) + P(\text{Body Diode})\} \times R_{th(c-f)} \\ & + \{P(\text{SiC-MOSFET}) + P(\text{Body Diode})\} \times R_{th(f-a)} + T_a \quad \text{---(30)} \end{aligned}$$

Additionally, the difference between the junction temperature and the ambient temperature, $\Delta T_{vj}(\text{SiC-MOSFET})$, is given as follows:

$$\begin{aligned} \Delta T_{vj} = & \{P(\text{SiC-MOSFET}) + P(\text{Body Diode})\} \times R_{th(j-c)}(\text{SiC-MOSFET}) \\ & + \{P(\text{SiC-MOSFET}) + P(\text{Body Diode})\} \times R_{th(c-f)} \\ & + \{P(\text{SiC-MOSFET}) + P(\text{Body Diode})\} \times R_{th(f-a)} \quad \text{---(31)} \end{aligned}$$

Here, the measurement points for the case temperature (T_c) and the heat sink temperature (T_f) correspond to the defined temperature measurement locations shown in Figure 3.14.

Please note that if the case temperature measurement location differs from this location, the thermal resistance value will differ from the value listed in the datasheet.

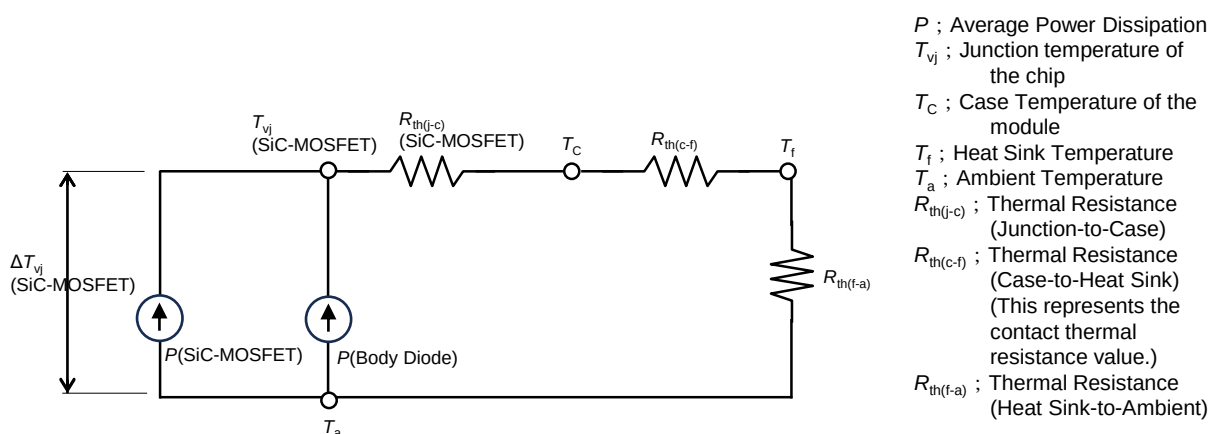


Figure 3.15 Thermal Equivalent Circuit

(1) Transient State

Generally, as described in the previous section, it is sufficient to consider the steady-state junction temperature (T_{vj}) using the average power dissipation. However, in actual applications, repetitive switching occurs, causing the power dissipation to take a pulsed form. When the junction temperature (T_{vj}) is considered relative to the case temperature (T_c), it exhibits a temperature ripple as shown in Figure 3.16. Under these conditions, assume the power dissipation is a continuous rectangular pulse train with a constant period and peak value. The peak junction temperature ($T_{vj(\text{peak})}$) can then be calculated using the following equation and the transient thermal resistance characteristic curve shown in Figure 3.17.

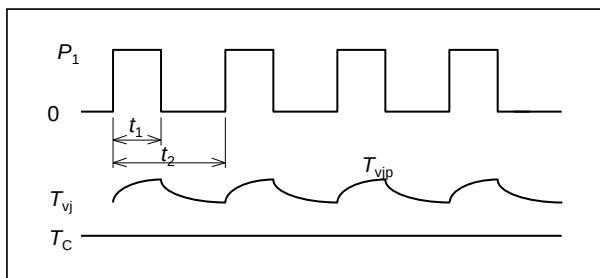


Figure 3.16 Temperature Ripple

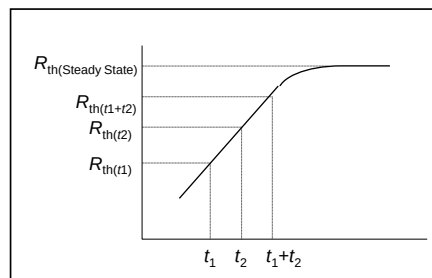


Figure 3.17 Transient Thermal Impedance

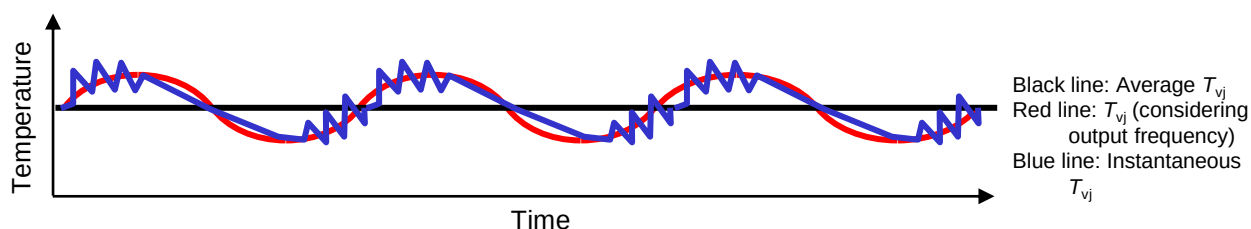


Figure 3.18 Temperature Ripple During Inverter Operation

Figure 3.18 shows the temperature ripple that occurs during inverter operation. The junction temperature oscillates at the output frequency, superimposed with the ripple at the carrier frequency. It is critical to ensure that the peak temperature—accounting for these oscillations—does not exceed the absolute maximum junction temperature ($T_{vj(\text{max})}$), even momentarily.

3-5-4. Precautions for Temperature Ripple and Temperature Fluctuations

(1) Considerations for Temperature Ripple

- Select a heat sink after performing the analysis described in the previous section, ensuring that the peak junction temperature ripple ($T_{vj(\text{ripple})}$) does not exceed the absolute maximum rating ($T_{vj(\text{max})}$).
- Large temperature ripples increase stress on the module's internal structural components. If this occurs over a large number of cycles, it poses a risk of reducing the module's operational lifetime.
- Note that time-varying power dissipation can cause the case temperature (T_c) to fluctuate due to contact thermal resistance between the case and the heat sink.

(2) Module Lifetime Curve under Power Cycle Mode

Power cycle capability is a key lifetime metric for operating modes where the cooling system and module case temperature (T_C) remain relatively stable, while the device junction temperature (T_{vj}) fluctuates. This curve illustrates the relationship between the magnitude of the device temperature change (ΔT_{vj}) and the number of cycles (N). It primarily represents a degradation mode where wire bonding connections experience stress, potentially leading to a shift in the on-state voltage ($V_{DS(on)}$).

The test method defines one cycle as passing the device's rated current for several seconds, followed by turning it off for several seconds, thereby inducing a change in junction temperature.

Note: In actual applications, contact thermal resistance between the module case and the heat sink is significant. Consequently, the case temperature (T_C) may also vary. Therefore, ΔT_{vj} should be evaluated considering the temperature difference relative to the heat sink (fin).

3-5-5. Concept of Power Cycle Lifetime in Actual Equipment

In railway traction inverters, power module operating conditions change dynamically according to the train's mission profile—specifically during starting, accelerating (powering), coasting, decelerating (regenerating), and stopping. Power losses resulting from these states cause repeated heating and cooling, leading to complex junction temperature (T_{vj}) fluctuations. These fluctuations impose a power cycle load on the module. Consequently, the product lifetime is primarily determined by the power cycle lifetime associated with these T_{vj} changes during actual operation. Field lifetime estimation requires determining operating conditions based on the train's actual mission profile.

Figure 3.19 Shows the Methodology for Determining the Actual Power Cycle Lifetime.

1. Mission Profile to Operating History: The inverter's operating history (current, voltage, modulation index, power factor, and switching frequency) is derived from the mission profile.
2. Loss Calculation: SiC-MOSFET power loss history is calculated using these values combined with I_D - V_{DS} , I_S - V_{SD} , and switching loss $E_{on}/E_{off}/E_{rr}$ characteristics.
3. Temperature Calculation: Junction temperature (T_{vj}) and case temperature (T_C) are calculated from the loss history and transient thermal impedance data.
4. Lifetime Estimation: Power cycle lifetime is estimated using the temperature swings (ΔT_{vj}) and cycle counts derived from this history.

Since the SiC-MOSFET T_{vj} waveform is typically complex and irregular, the rainflow counting algorithm is employed to convert the waveform into a set of ΔT_{vj} values and their respective cycle counts.

Figure 3.20 Shows This Conversion Process:

- (a) Shows a sample temperature history.
- (b) The rainflow algorithm decomposes the total history into four distinct ΔT_{vj} cycles.
- (c) & (d) Specifically, the waveform is decomposed into a large+ ΔT_{vj1} (blue) and a small- ΔT_{vj2} (red), followed by a large- ΔT_{vj3} (yellow) and a small+ ΔT_{vj4} (light blue).

The power cycle lifetime (N) is a function of ΔT_{vj} , the maximum temperature (T_{vjmax}), and the on-time (t_{on}), expressed as:

$$N = N_0 (\Delta T_{vj})^n \cdot t_{on}^m \cdot \exp\left(\frac{Q}{k_B(273+T_{vjmax})}\right) \quad \text{---(33)}$$

n, m : constants, Q : Activation energy (eV), k_B ; Boltzmann constant 8.6173×10^{-5} (eV/K)

This model is used to calculate the cumulative damage (D) using the power cycle lifetime prediction formula (Eq. 33). The actual power cycle lifetime (N) is then determined as the number of cycles at which $D = 1$. This is calculated as follows:

$$D = \sum_{i=1}^n \left(\frac{1}{N_i} \right) = \sum_{i=1}^n \left(\frac{1}{N_0 (\Delta T_{vj,i})^n \cdot t_{ON,i}^m \cdot \exp\left(\frac{Q}{k_B(273+T_{vjmax,i})}\right)} \right) \quad \text{---(34)}$$

$$N = \frac{1}{D} \quad \text{---(35)}$$

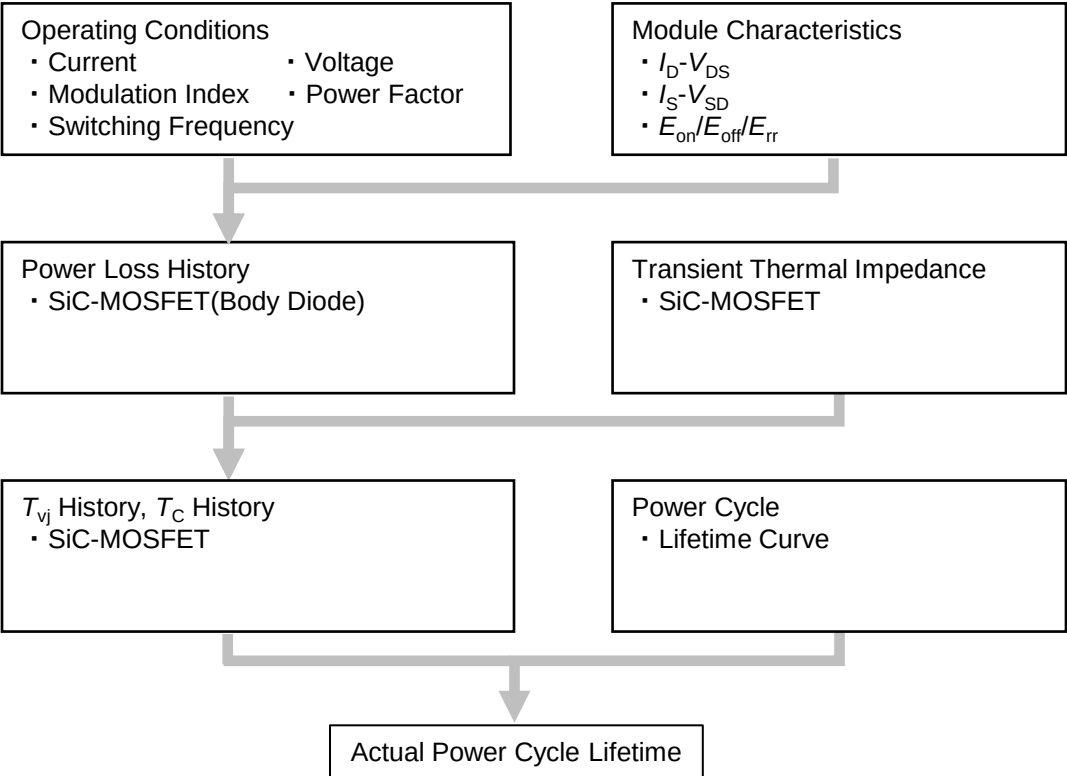


Figure 3.19 Method for Calculating Actual Power Cycle Lifetime

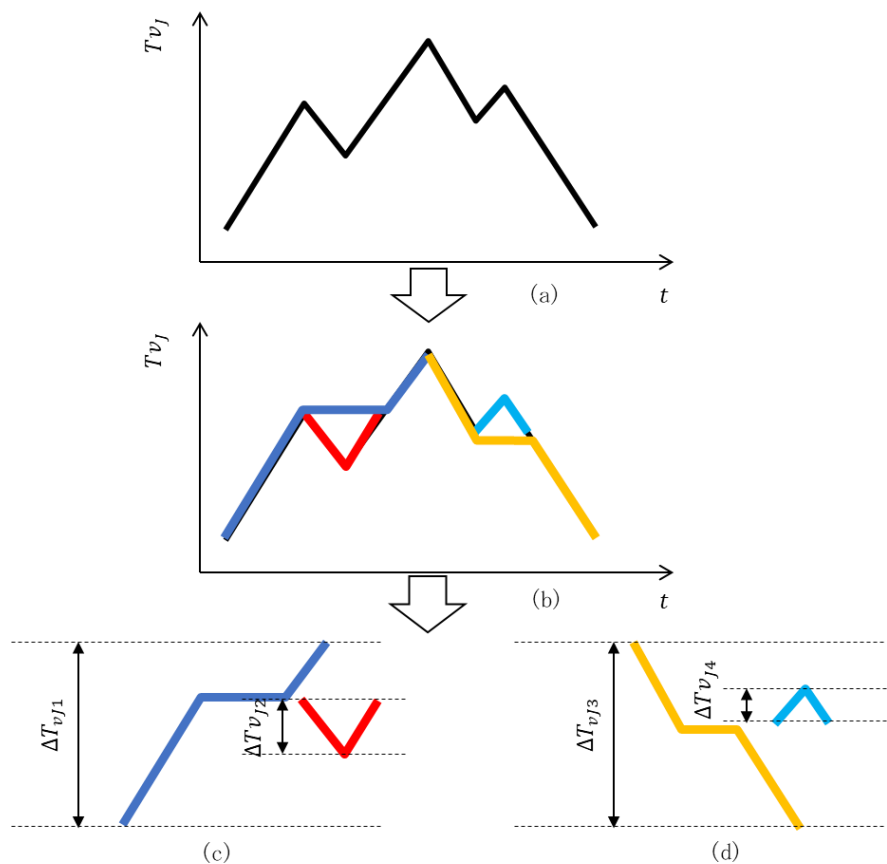


Figure 3.20 Estimation of Actual Power Cycle Lifetime : rainflow Algorithm

3-5-6. Temperature Monitoring of Power Modules Using Thermistors

Power modules equipped with an NTC (Negative Thermal Coefficient) thermistor allow for temperature monitoring during operation. The relationship between the NTC thermistor resistance (R) and its absolute temperature (T_r) is approximated by the following exponential function:

$$R = R_0 \cdot \exp\left(B \left(\frac{1}{T_r} - \frac{1}{T_0}\right)\right) \quad \text{---(36)}$$

Here, B is the B-constant representing the temperature dependence of the thermistor's resistance, and R_0 is the resistance at the reference temperature T_0 .

Using Equation (36), the thermistor temperature can be determined by measuring the resistance. However, since this equation is an approximation, referring to the R - T characteristic curve in Figure 3.21 provides more accurate temperature measurements.

Note that the thermistor is mounted physically apart from the SiC-MOSFET chip. Consequently, the thermistor temperature (T_r) differs from the junction temperature (T_{vj}). Because the correlation between T_{vj} and T_r varies with operating conditions, the thermistor is unsuitable for estimating T_{vj} . Specifically, it cannot be used for protection against overheating induced by short-duration loads.

Under general operating conditions, the relationship between thermistor temperature (T_r), junction temperature (T_{vj}), and case temperature (T_c) is as follows:

$$T_c < T_r < T_{vj} \quad \text{---(37)}$$

Furthermore, under general operating conditions, the relationship $T_c \approx T_r$ holds true in the steady state. Therefore, the thermistor can be used to detect a sustained rise in case temperature (T_c) caused by abnormalities in the thermal grease, heat sink, or cooling water.

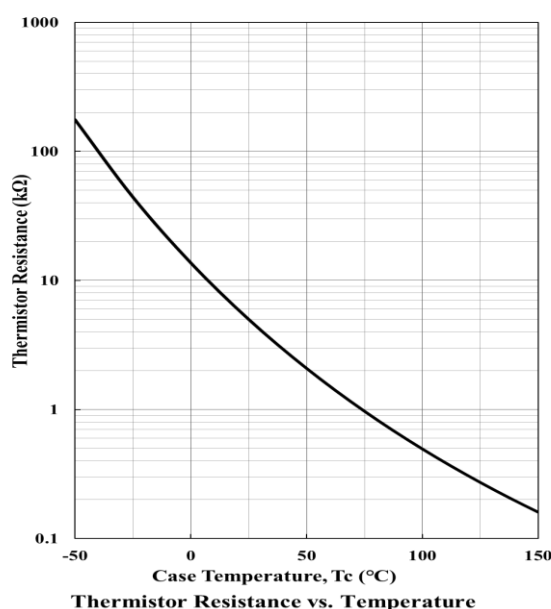


Figure 3.21 Relationship Between NTC Thermistor Resistance and Temperature : typical

3-6. PROTECTION CIRCUIT

3-6-1. Short-circuit and Overcurrent Conditions

(1) Arm Short Circuit

Figure 3.22 shows the schematic waveforms of the SiC-MOSFET short-circuit test. If the device enters a short-circuit state due to a system anomaly, the SiC-MOSFET drain current (I_D) increases rapidly. Since SiC-MOSFETs have a very high saturation current, the large current generated during a short circuit can cause thermal destruction of the device. The duration that the SiC-MOSFET can withstand the current without suffering destruction is defined as the “short-circuit capability” (t_{sc}). The gate drive circuit must ensure that the delay time from short-circuit detection to protection circuit shutdown is shorter than this capability. The short-circuit capability depends on V_{DS} , V_{GS} , and T_{vj} . Generally, the higher the supply voltage V_{DD} , gate voltage (V_{GS}), or junction temperature (T_{vj}), the shorter the capability becomes.

Note: An arm short circuit occurs if the device (SiC-MOSFET) fails or if ON signals are input to both the upper and lower arms simultaneously.

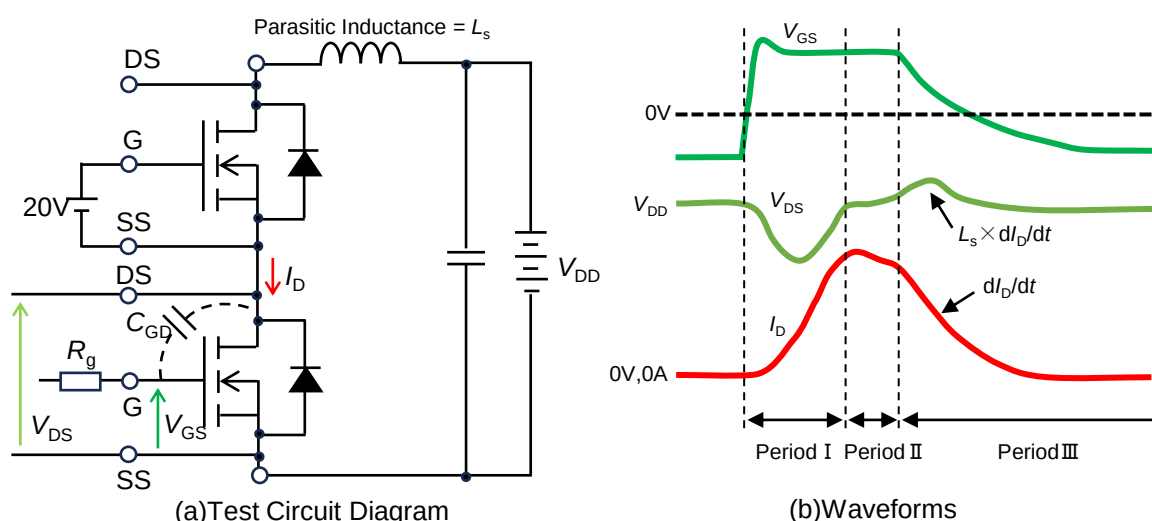


Figure 3.22 Schematic Waveforms of the SiC-MOSFET Short-circuit Test

The waveform is broadly divided into three periods.

Period I : The SiC-MOSFET turns on, and current begins to flow. V_{DS} drops initially due to the parasitic inductance (L_S) and high dI_D/dt . As dI_D/dt decreases, V_{DS} rises, generating a steep dI_D/dt . This dI_D/dt causes current to flow from the drain to the gate via C_{GD} , causing V_{GS} to temporarily exceed the gate supply voltage. This phenomenon results in an increase in drain current I_D , creating a peak. Ensure that the gate voltage at this time does not exceed the absolute maximum gate voltage rating. Since dI_D/dt depends significantly on the turn-on gate resistance, careful consideration is required when setting the value.

Period II : Due to the self-heating of the SiC-MOSFET, T_{vj} increases over time, causing I_D to decrease.

Period III : When the gate voltage is turned off, a surge voltage of $L_S \times di_D/dt$ is generated. If the current is interrupted using the standard turn-off gate resistance, this surge voltage may be high enough to exceed the RBSOA. Therefore, we recommend setting the turn-off gate resistance used upon short-circuit detection to a value larger than the standard turn-off resistance value.

(2) Output Short Circuit and Ground Fault

Figure 3.23 shows the current paths for an output short circuit and a ground fault. An output short circuit occurs if the motor fails, or if the control or gate circuit malfunctions and becomes stuck in a specific state in a particular phase.

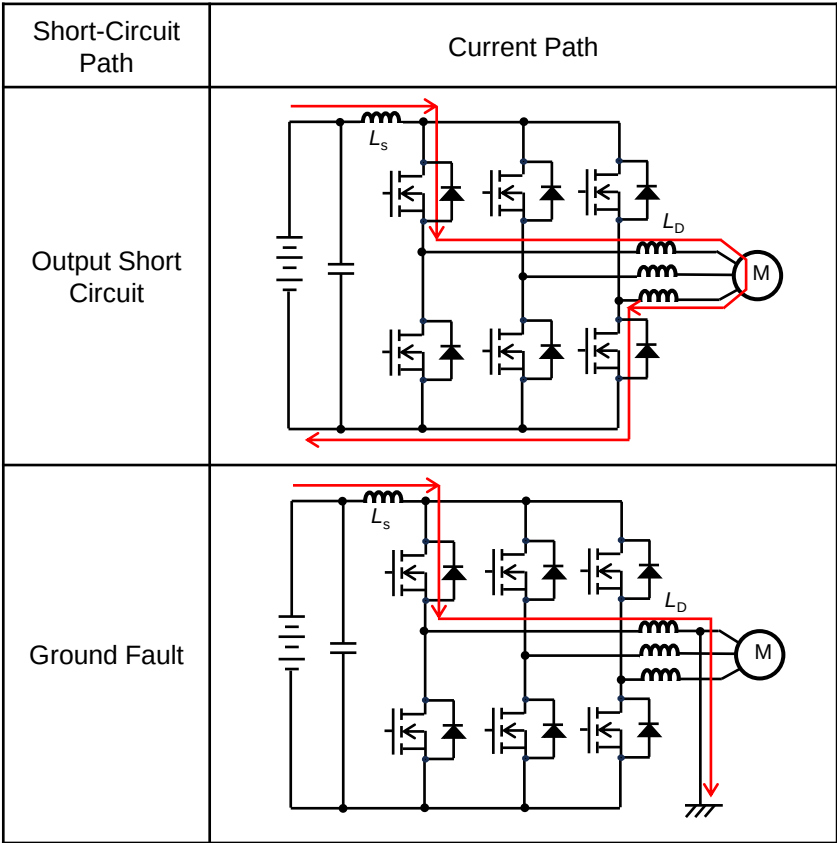


Figure 3.23 Current Paths for Output Short Circuit and Ground Fault

Figure 3.24 shows the simulation test circuit and waveforms for an output short circuit. In this fault condition, the short-circuit path comprises the parasitic inductance (L_S) between the smoothing capacitor and the module, as well as the motor winding inductance and the wiring inductance (L_D) connecting the inverter and the motor.

Assuming the inductance of the short-circuit path is

$$L_{sh}=L_S+L_D \quad \text{---(38)}$$

the current rise rate di/dt is expressed as

$$di/dt=V_{DD}/L_{sh}(\text{A/sec}) \quad \text{---(39)}$$

where V_{DD} is the supply voltage. If the time elapsed since the start of the short circuit is t (sec), the drain current I_D becomes

$$I_D=di/dt \times t(\text{A}) \quad \text{---(40)}$$

When I_D reaches the saturation current, the drain voltage V_{DS} increases. Similar to an arm short circuit, this results in significant power dissipation (heat generation) because the saturation current flows while the high supply voltage V_{DD} is applied across the SiC-MOSFET.

On the other hand, a ground fault in the motor or the cable between the inverter and the motor results in a waveform similar to that shown in Figure 3.24.

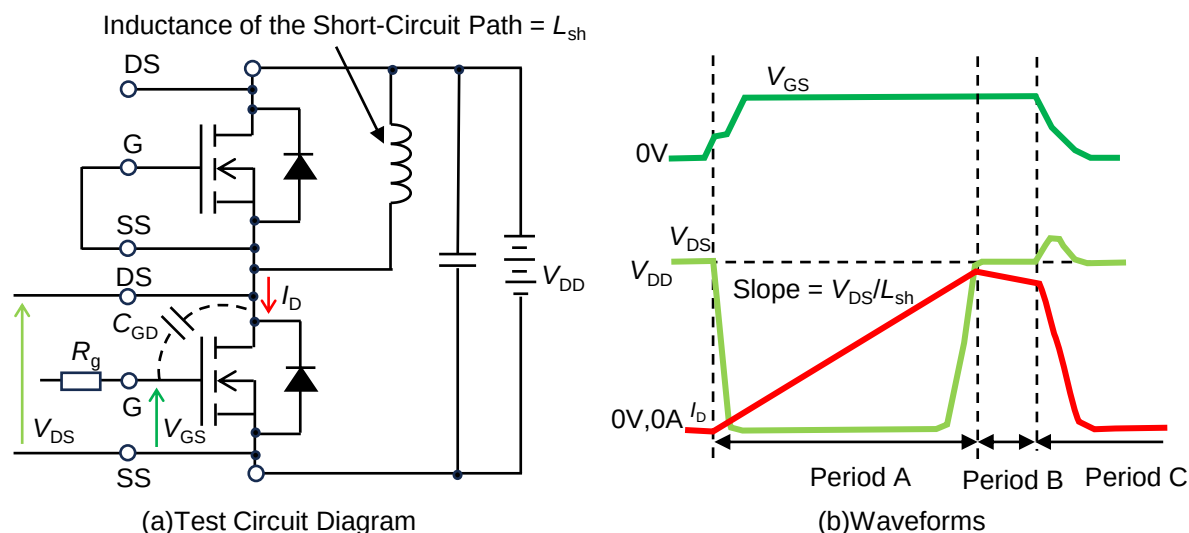


Figure 3.24 Output Short-Circuit Simulation Test Circuit and Waveforms

3-6-2. Overvoltage

(1) Cause of Overvoltage

During SiC-MOSFET turn-off or diode recovery, the rapid change in current (di/dt) induces a surge voltage across the wiring inductance (L_S) between the module and the smoothing capacitor. The magnitude of this surge is $L_S \times di/dt$. The peak turn-off voltage (V_{DP}) can be expressed using the following equation, where V_{DD} is the DC supply voltage:

$$V_{DP}=V_{DD}+ di/dt \times L_S \quad \text{---(41)}$$

Please verify that the voltage and current trajectories (locus) remain within the RBSOA and RRSOA limits under the system's maximum DC voltage conditions.

(2) Methods for Suppressing Surge Voltage

The following methods are effective for suppressing surge voltage:

- (a) Reduce di/dt by adjusting the gate resistance or negative gate bias of the SiC-MOSFET drive circuit. (For details, please refer to Section 3-2, "Gate Drive Circuit".)
- (b) Place the DC-link capacitor (smoothing capacitor) as close as possible to the SiC-MOSFET module. Additionally, use capacitors with low internal inductance (ESL), such as film capacitors.
- (c) To reduce parasitic inductance (L_s), use thick and short busbars for wiring. It is also effective to use a laminated busbar structure for the P and N lines.

(3) Examples of Surge Voltage Characteristics

Figure 3.25 illustrates the surge voltage characteristics relative to drain current during SiC-MOSFET turn-off and diode recovery.

The SiC-MOSFET turn-off surge voltage (V_{DSP}) increases as the drain current (I_D) increases. Conversely, the diode recovery surge voltage (V_{AKP}) tends to be higher at lower current levels. As described, surge voltage varies depending on voltage/current conditions, gate drive parameters, temperature, and circuit layout. Therefore, ensure that operation remains within the RBSOA and RRSOA limits specified in the datasheet under all expected system operating conditions.

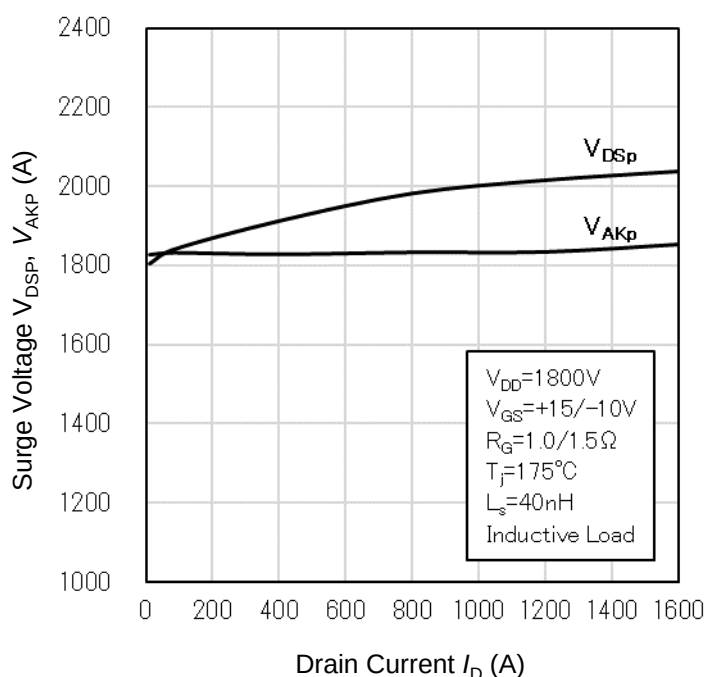


Figure 3.25 Drain Current Dependence of the Surge Voltage during SiC-MOSFET turn-off and Diode Recovery : Example

CHAPTER 4. MOUNTING PRECAUTIONS

4-1. MOUNTING SiC-MOSFET MODULES ONTO HEAT SINKS

4-1-1. Recommended Tightening Torque

TABLE 4.1 Shows the Recommended Torque Values for Both Temporary Tightening and Final Tightening.

TABLE 4.1 Recommended Tightening Torque for SiC-MOSFET Module Mounting

No	Screw Size	Rated Torque (N·m)	Recommended Torque (N·m)	Temporary Tightening Torque (N·m)	Final Tightening Torque (N·m)
1	M6	6.0	5.5	1.5~2.0	5.0~6.0

4-1-2. Application of Thermal Grease and Module Mounting Method

(1) Purpose

Establishing a proper thermal interface is critical when mounting a power module to a heat sink. Thermal grease is widely used as a thermal interface material (TIM) to minimize the contact thermal resistance between the power module and the heat sink. To achieve an effective thermal interface, the grease must be applied correctly. Improper application may cause the chip to overheat, potentially leading to catastrophic module failure.

(2) Application Method

This section outlines a mounting method for heat sinks that has been verified by our company. Note that the optimal mounting method varies depending on the heat sink geometry. Therefore, this information is provided for reference only and does not guarantee the final mounting results. Figure 4.1 illustrates the workflow, and Figure 4.2 shows an example of the stencil mask pattern used in the process.

Step1 : Set the Stencil Mask

Remove foreign matter and debris from the baseplate surface and set the stencil mask on the baseplate as shown in Fig. 4.1(a).

Step2 : Apply Grease

As shown in Fig. 4.1(b), apply grease to the edge of the stencil mask in an amount sufficient to spread across the entire surface of the baseplate.

Step3 : Spread the Grease

As shown in Fig. 4.1(c), use a squeegee to push the grease into the stencil mask apertures. Fig. 4.1(d) shows the state of the grease after spreading.

Step4 : Remove the Stencil Mask

Remove the stencil mask after the spreading process is complete, as shown in Fig. 4.1(d).

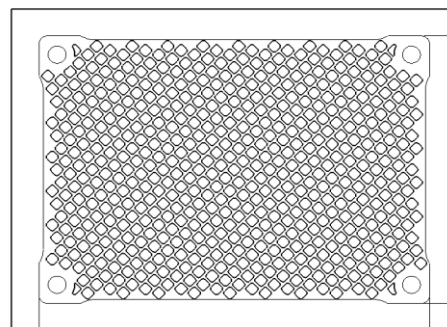
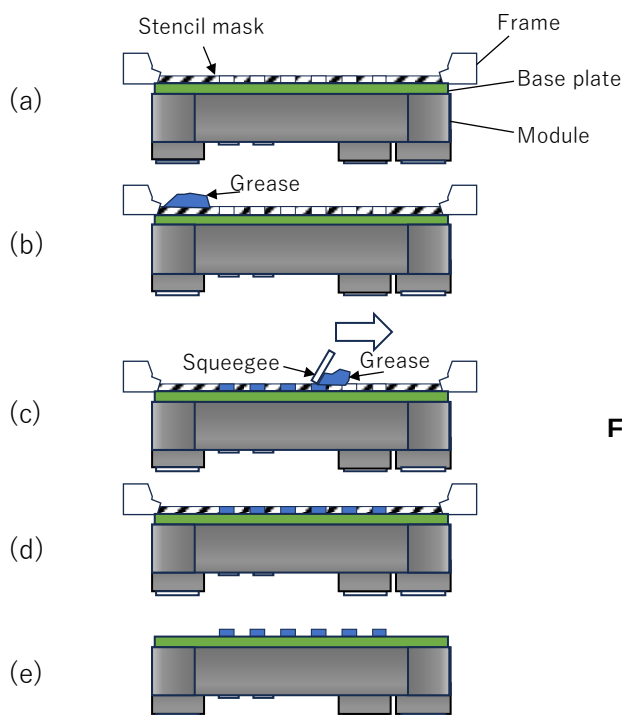


Figure 4.2 An Example of Stencil Mask Pattern

Figure 4.1 Thermal Grease Application Workflow

For the evaluation method of thermal grease, please contact our sales department.

4-1-3. Recommended Screw Tightening Sequence

For temporary and final tightening of 4-point mounting modules, please tighten in the order shown in Figure 4.3.

Temporary Tightening; Order of 1 $\Rightarrow$ 2 $\Rightarrow$ 3 $\Rightarrow$ 4 ...

Final Tightening; Order of ... 4 $\Rightarrow$ 3 $\Rightarrow$ 2 $\Rightarrow$ 1

Note that the tightening sequence should follow a diagonal pattern, and there are no specific restrictions on the starting position.

(The same applies to retightening.)

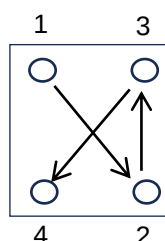


Figure 4.3 Screw Tightening Sequence of SiC-MOSFET

4-1-4. Surface Roughness and Warpage of the Heat Sink

Important Notice

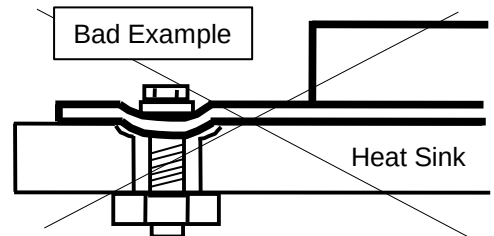
- (1) Maintain a heat sink surface roughness of "25S" ($Rz \approx 25\mu\text{m}$) or smoother.
- (2) Keep the heat sink flatness (warpage) within $50\mu\text{m}$ per screw hole pitch, encompassing both concave and convex distortions.
- (3) Remove any burrs from the heat sink surface and ensure that the screw holes are chamfered.
- (4) Ensure that the interface is free of foreign matter, such as cutting debris (swarf), between the SiC-MOSFET module and the heat sink.

4-1-5. Module Mounting Holes on the Heat Sink

If the heat sink mounting hole diameter is excessive, the SiC-MOSFET module baseplate may deform as shown in Figure 4.4, potentially damaging the internal dies (chips). Therefore, ensure that the mounting hole diameter is appropriate for the screw size. TABLE 4.2 lists the recommended values for mounting hole diameters and chamfer dimensions.

TABLE 4.2 Recommended Values for the Mounting Hole Diameter and Chamfering Dimensions (mm)

No	Screw Size	Mounting Hole Diameter	Recommended Chamfering Value
1	M6	$\Phi 7.5$	C0.5



If the mounting hole diameter is too large, the metal base plate of the SiC-MOSFET module will deform.

Figure 4.4 Example of Improper Mounting on a Heat Sink

4-2. TERMINAL INSTALLATION

4-2-1. Terminal Installation

(1) Terminal Mechanical Load Limits

Figure 4.5 Shows the Maximum Allowable Loads for the nHPD2 Package Terminals.

- Main Terminals: Do not apply tensile or lateral loads exceeding 50 N/terminal, or compressive loads exceeding 250 N/terminal.
- Moment Loads: Do not apply rotational moments or unbalanced loads to the terminals.
Note that applying force to the far end of an attached busbar generates a large moment proportional to the busbar length, which can damage the package.
- Handling: Do not pull or repeatedly bend the main or auxiliary terminals, as this may cause terminal fracture or internal wire bond breakage.

(2) Static vs. Dynamic Loads

The specified limits apply only to a single static load occurring during busbar assembly.

They do not cover repetitive loads caused by thermal expansion or vibration.

- Ensure that mechanical stress and vibration are not transmitted to the terminals during operation.
- Do not use the terminals to support the weight of heavy components (e.g., heavy busbars), as this may lead to fatigue failure. Validate the design via vibration testing on the actual unit.

Prohibition of Lubricants:

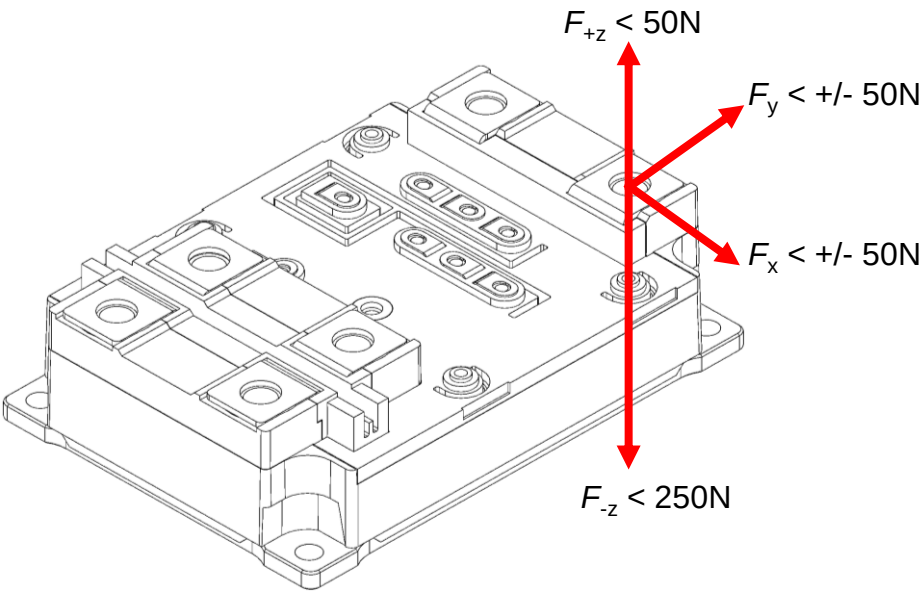
Do not use lubricants at the terminal-to-busbar interface. Reduced friction may cause the terminal to rotate when tightening the screw, potentially resulting in internal connection failure or package damage.

4-2-2. Recommended Screw Tightening Sequence

There are no specific regulations regarding the screw tightening sequence for the terminal section.

4-2-3. Screw Tightening Method

Install the device using a manual or electric torque driver (or torque wrench) at the recommended torque specified in TABLE 4.3. Ensure that the screw surfaces are clean and dry (unlubricated). Never use impact wrenches or impact drivers.



Do not apply an eccentric load to each of the two terminals.
Do not apply any moment (rotational force) to the terminals.

Figure 4.5 Maximum Allowable Load on the Terminals

TABLE 4.3 Mounting Torque for Screw Terminals

No	Screw Size	Rated Torque (N · m)	Recommended Torque (N · m)	Minimum Torque (N · m)	Remarks
1	M3	0.8	0.65	0.5	Auxiliary terminals
2	M8	15.0	15.0	12.0	-

4-2-4. Recommended Screw Depth

Figure 4.6 illustrates the cross-section of the screw-type mounting interface. Please select a screw length such that the protrusion length ‘d’ (the length extending beyond the nut) is between 1 mm and 2 mm.

The dimensions (a, b and c) shown in Figure 4.6 correspond to the screw types listed in TABLE 4.4. Note that these dimensions exclude the thickness of wiring and other external components.

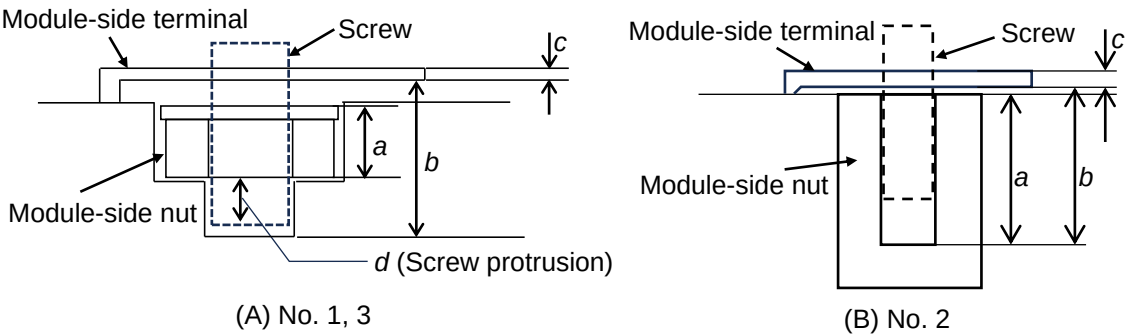


Figure 4.6 Cross-sectional Views of Module Screw Holes

TABLE 4.4 Screw Hole Dimensions
(Package Type : nHPD2) (Ref. Figure 4.6 dim. a, b, and c)

No.	Screw Size	a(mm)	b(mm)	c(mm)	Remarks
1	M3	24	5.5	0.5	S2main, T, D1AUX, D2AUX
2	M3	6.5	6.5	0.5	G2, S2AUX, S1AUX, G1
3	M8	8.0	15.0	1.5	

4-3. DESIGN REFERENCE FOR BUSBAR AND CAPACITOR CONNECTION

When connecting DC-link capacitors to the power module terminals via busbars, it is critical to minimize the parasitic inductance of the busbars. Excessive inductance causes a significant increase in turn-off surge voltage, creating a risk of exceeding the module’s rated voltage (V_{DSS}). Strictly ensure that the peak voltage across the terminals, including the surge component, never exceeds the rated V_{DSS} under any operating condition.

Additionally, note that switching losses are influenced by the busbar geometry and may differ from the typical values specified in the datasheet

Therefore, characteristics must be measured in the actual inverter configuration. Figure 4.7 illustrates an example of connecting busbars and capacitors to the nHPD2 package. In this example, the parasitic inductance is minimized by employing a laminated structure for the DC busbars. Note that we utilize a similar busbar design during our in-house product characterization.

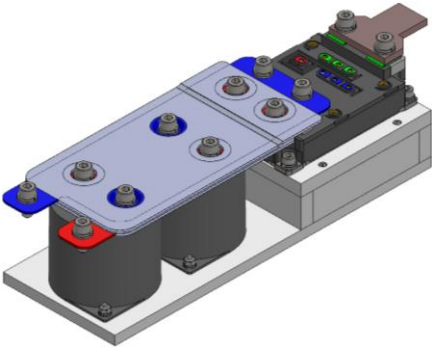


Figure 4.7 Example of Connecting Busbars and Capacitors to the Power Module

4-4. BUSBAR INSTALLATION PRECAUTIONS

(1) Terminal Handling

Do not lift, bend, or pull the main or auxiliary terminals, as this may damage the terminal structure. Furthermore, avoid system designs where the terminals bear significant mechanical loads, as excessive stress causes damage. Validate the mechanical design beforehand via vibration testing on the actual system.

(2) Tightening Procedure

TABLE 4.3 lists the recommended tightening torques. When connecting multiple terminals to a common busbar, use a two-step tightening process:

1. Provisionally tighten all screws to approximately 30% of the recommended torque.
2. Proceed to the final tightening at the full recommended torque.

When removing the busbar, reverse this sequence: loosen all screws to the provisional level before fully removing any single screw. "One-sided tightening" (applying full torque to one screw while others are loose) exerts excessive stress and may crack the module case.

(3) Busbar Installation & Support

Figure 4.8 illustrates a recommended busbar connection. Secure the busbar to a support post near the terminals to prevent stress transmission. Ensure that tightening/loosening torque and external forces are not applied directly to the module case. Excessive stress can lead to case fractures or internal connection failures (e.g., short circuits or wire bond breakage).

•Design Note: Design the busbar support so that a compressive load—rather than a tensile load—is applied to the module terminals.

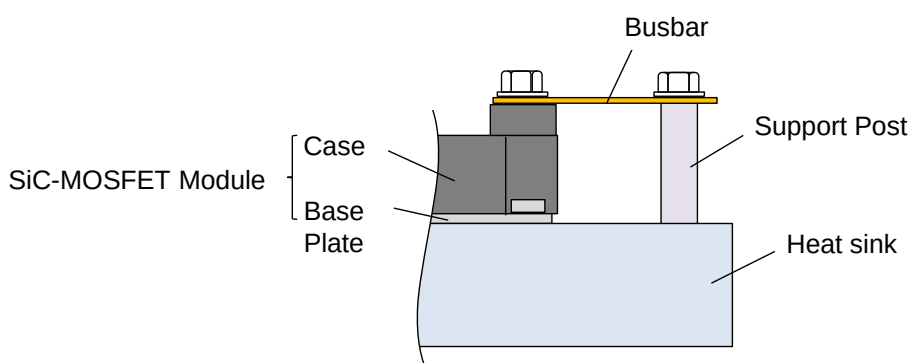


Figure 4.8 Example of a Busbar Connection

During operation, current flowing through the main terminals generates heat (Joule heating). A portion of this heat is dissipated through the connected busbars, causing the temperature at the terminal interface to rise.

Consequently, inverter designs must account for the impact of this heat dissipation and temperature rise on the reliability of the busbars and surrounding components.

Figure 4.9 shows the relationship between terminal heat dissipation and the temperature difference (rise). Specifically, it presents data for sinusoidal currents of 1600 A_{peak} and 800 A_{peak} applied to the AC terminal.

Furthermore, depending on operating conditions, the hottest point (hotspot) of the main terminal may be located internally within the package, rather than at the connection surface. Therefore, during high-current operation, limits are specified for both the busbar connection temperature and the case temperature to prevent internal overheating

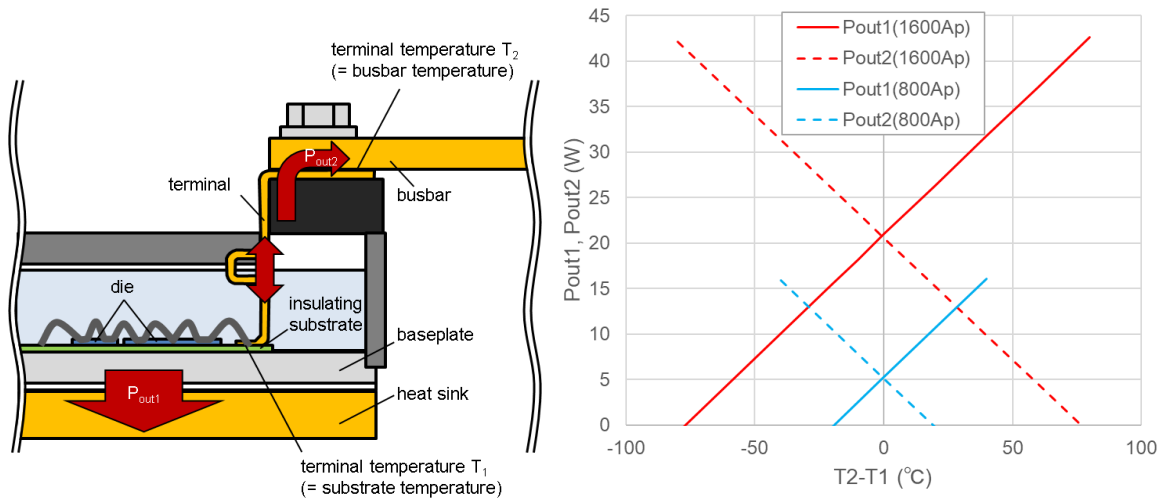


Figure 4.9 Relationship between the amount of heat dissipated from the main terminal and the temperature difference across the terminal

4-5. PCB MOUNTING

PCB Mounting Torque & Sequence TABLE 4.5 specifies the recommended tightening torque for mounting the PCB to the module. Figure 4.10 illustrates the required tightening sequence.

Procedure:

1. Tighten the four corner screws (A to D) in the order shown.
2. Tighten the remaining inner screws (4 to 11) in any order.

Screw Selection: The screw hole depth is specified in the datasheet outline drawing. Select an appropriate screw length by accounting for the PCB thickness and the effective thread depth.

TABLE 4.5 Recommended Tightening Torque for PCB Mounting Terminals

No	Screw Diameter	Rated Torque (N·m)	Recommended Torque (N·m)
1	M3	0.8	0.65±0.15

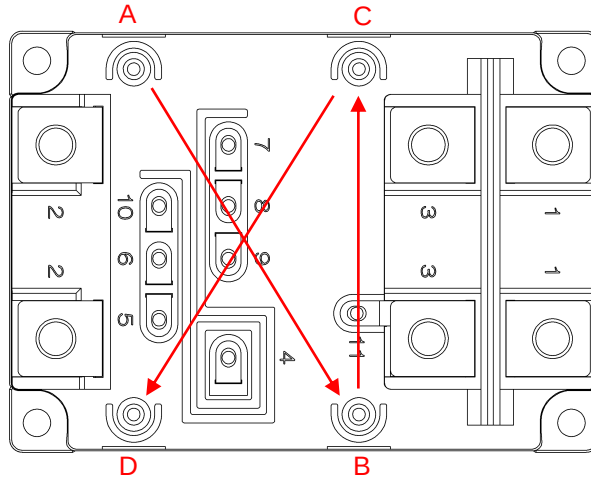


Figure 4.10 Tightening Sequence for the PCB Mounting Screws

4-6. INSTALLATION ENVIRONMENT

Important

Please observe the following precautions regarding the installation environment:

- **Corrosive Atmospheres:** Avoid using the module in atmospheres containing corrosive gases. These gases can degrade contact reliability and heat dissipation performance. Note that exposure may also cause discoloration of the terminals or the metal baseplate.
- **Water Exposure:** Ensure that the SiC-MOSFET module is protected from rain, water droplets, and moisture.

4-7. STORAGE AND TRANSPORTATION PRECAUTIONS

Important

(1) Store the modules under the following conditions:

- **Temperature :** 40 °C or less
- **Humidity :** 60% RH or less
- **Dust :** Avoid locations subject to excessive dust accumulation. Conductive dust can cause short circuits.
- **Corrosive Gases:** The environment must be free from corrosive gases such as sulfur dioxide and chlorine gas.
- **Static Electricity Protection (ESD):** Do not remove the conductive shorting clip (metal piece) attached to the gate and source signal terminals until immediately before wiring. This clip protects the device from electrostatic discharge.

(2) Transport and Handling Precautions

- **Handle with Care:** Handle the modules with care during transport and handling. Do not throw or drop the units, as this may cause internal device damage. Never use any device that has been dropped or subjected to excessive mechanical shock.
- **Shipping Marks:** Adhere to all instructions and symbols marked on the shipping box, such as "Handle with Care" or "Fragile." Handle the packages in a manner that avoids mechanical vibration and shock.
- **Moisture Protection:** Take measures to prevent the shipping box from being exposed to rain or water. Keep the packaging dry at all times.

4-8. ESD PRECAUTIONS (ELECTROSTATIC DISCHARGE)

Important

SiC-MOSFETs feature a delicate MOS gate structure. Strictly adhere to the following ESD countermeasures:

- **Shorting Clip:** Do not remove the conductive shorting clip (or conductive foam) connecting the gate and source terminals until immediately before wiring/assembly.
- **Personnel Grounding:** Operators handling the device must be grounded via a wrist strap containing a high-resistance resistor (approx. 100 k Ω to 1 M Ω). Handle the device by the package case; avoid direct contact with the gate terminal.
- **Equipment Grounding:** Ensure that workbenches, soldering irons, and all equipment contacting the device are properly grounded.
- **Testing:** Discharge all residual charge from measuring instruments before connection. When applying voltage, ramp up from 0 V and ramp down to 0 V before disconnecting.

4-9. CIRCUIT LAYOUT AND WIRING METHODS FOR SiC-MOSFET MODULES

(1) Main Circuit Wiring

Optimize the layout to minimize parasitic wiring inductance from the power supply. Excessive inductance causes high voltage surges during switching, which may lead to overvoltage breakdown of the SiC-MOSFET module. We recommend using laminated busbars to reduce this inductance. Ensure that the total commutation loop inductance (comprising the module, busbar, and capacitor) is lower than the value specified in the "Test Conditions" under "ELECTRICAL CHARACTERISTICS" in the datasheet.

(2) Gate Circuit Wiring

Keep the wiring between the gate driver and the SiC-MOSFET module as short as possible. Excessive wire length delays gate voltage rise and fall times, slowing switching speeds and making the circuit more susceptible to induced noise. Using twisted-pair or shielded wires is effective for reducing inductance and improving noise immunity.

4-10. MEASUREMENT PRECAUTION

(1) Measurement of V_{DSS}

When measuring V_{DSS} , ensure that the control gate and source terminals are short-circuited. Applying voltage with the gate floating (open) may damage the MOSFET. If condensation is suspected (e.g., following a heat cycle test), dry the module at approximately 100 °C for at least 2 hours before measuring under the specified conditions.

(2) Influence of Internal Inductance

Due to parasitic inductance in the internal wiring between the die (chip) and the module terminals, the voltage at the terminals differs from the actual voltage across the die during switching. This discrepancy arises from the induced voltage $L_s \times di/dt$, where L_s is the internal stray inductance and di/dt is the current rate of change. Consequently, at turn-on, the module terminal voltage is higher than the die voltage. Conversely, at turn-off, the voltage applied to the die exceeds the module terminal voltage.

The internal inductance of the nHPD2 package is approximately 10nH. Ensure that the peak voltage applied to the chip—calculated as $V_{supply} + L_s \times di/dt$ —does not exceed the device's rated voltage.

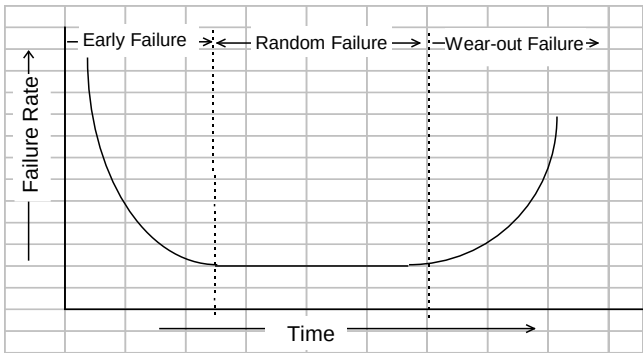
CHAPTER 5. RELIABILITY

This section explains general concepts and terminology regarding reliability.

It also describes the reliability test items and details specific to the module structure.

5-1. FAILURE RATE

Generally, the failure rate of semiconductor devices changes over time, as shown in Figure 5.1.



Early Failure: Failures occurring relatively early in use due to design/manufacturing defects or operating environment mismatches.

Random Failure: Failures occurring randomly after the early failure period and prior to the wear-out period.

Wear-out Failure: Failures where the failure rate increases over time due to fatigue, wear, degradation phenomena, etc.

Figure 5.1 Semiconductor Device Failure Rate (bathtub Curve)

5-2. FAILURE FACTORS

Factors determining the failure susceptibility of semiconductor components can be divided into internal factors (manufacturing-related) and external factors (usage-related), as shown in TABLE 5.1 below. If specific failures such as those shown in the table occur, please analyze the causal factors and implement appropriate countermeasures regarding the external factors.

TABLE 5.1 Causes of Failure

Factor Category		Specific Examples of Failure
Internal Factors	Factors determined by component materials and structure	(1) Intermetallic compound formation failure (Purple Plague) (2) Mismatch of Coefficient of Thermal Expansion (CTE)
	Factors caused by manufacturing process variations	(1) Internal bonding wire defects (e.g., misplacement, inadequate bonding pressure, surface scratches) (2) Scratches on the chip surface pattern (3) Die attach defects (e.g., soldering voids, delamination)
External Factors	Thermal Stress	(1) Wear-out degradation or failure due to thermal expansion (2) Acceleration of chemical changes (e.g., compound formation)
	Electrical Stress	(1) Dielectric breakdown (Package) (2) Dielectric breakdown (For chips with MOS structure)
	Mechanical Stress	(1) Terminal breakage (2) Package cracking (3) Insulation failure due to physical damage (Package)
	Chemical Stress	Corrosion of external electrodes
	Radiation	Characteristic changes due to surface charge accumulation

5-3. RELIABILITY TEST

To ensure the high reliability of our SiC-MOSFET modules, we conduct various reliability tests. The following table shows examples of typical test items we perform. Please note that actual test items and conditions may vary depending on the specific product model and specifications. For detailed reliability data, please refer to the delivery specifications or test reports of the respective products.

TABLE 5.2 Examples of typical reliability test items

Category	Typical test items
Environmental tests	High temperature storage test Low temperature storage test Temperature cycling test High humidity high temperature reverse bias test
Mechanical tests	Vibration test (variable frequency / fixed frequency) Mechanical shock test Mounting stress test Terminal strength test
Endurance tests	High temperature reverse bias test (AC/DC) High temperature gate bias test (AC) Thermal fatigue test Power cycling test

5-4. QUALITY ASSURANCE SYSTEM

Figure 5.2 Illustrates Our Quality Assurance System.

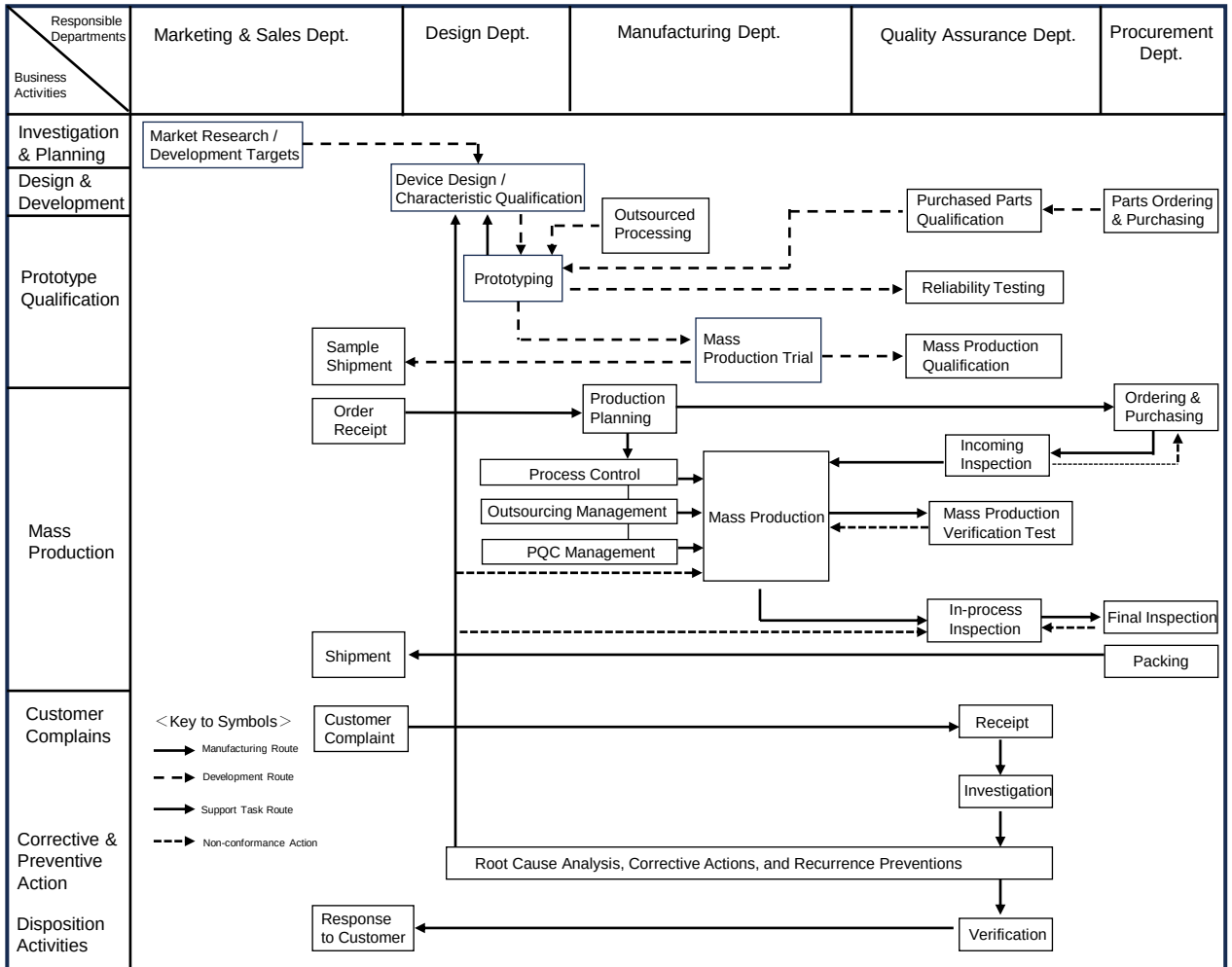


Figure 5.2 Quality Assurance System Diagram

CHAPTER 6. TROUBLESHOOTING

6-1. FAILURE MODES OF SiC-MOSFET MODULES (ELECTRICAL FAILURE MODES)

When investigating a SiC-MOSFET failure, refer to the fault tree below for root cause analysis.

Please note that this tree serves as a troubleshooting guide and may not identify the exact root

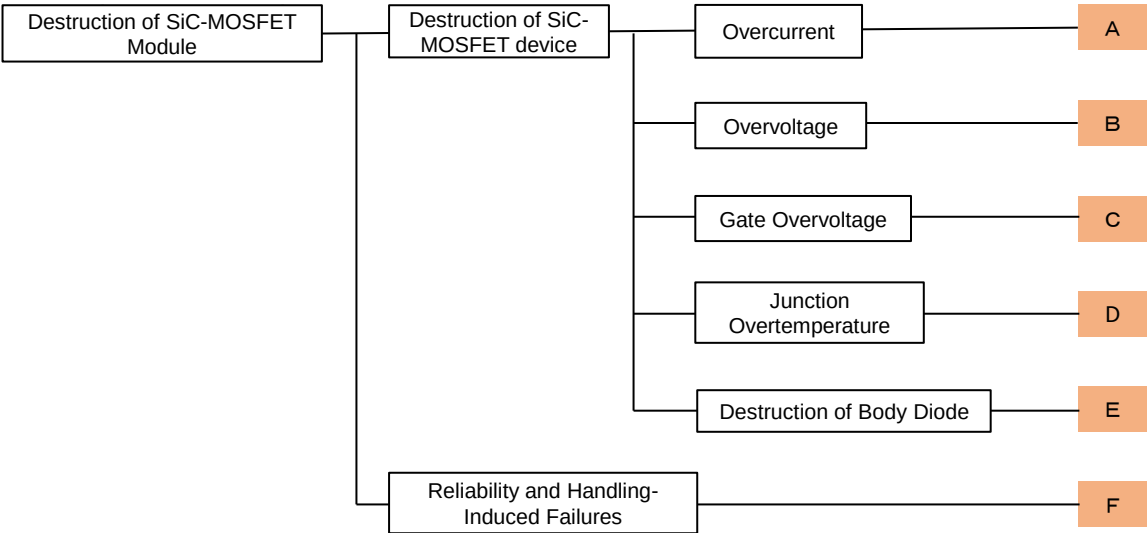


Figure 6.1 Failure Modes of SiC-MOSFET Modules

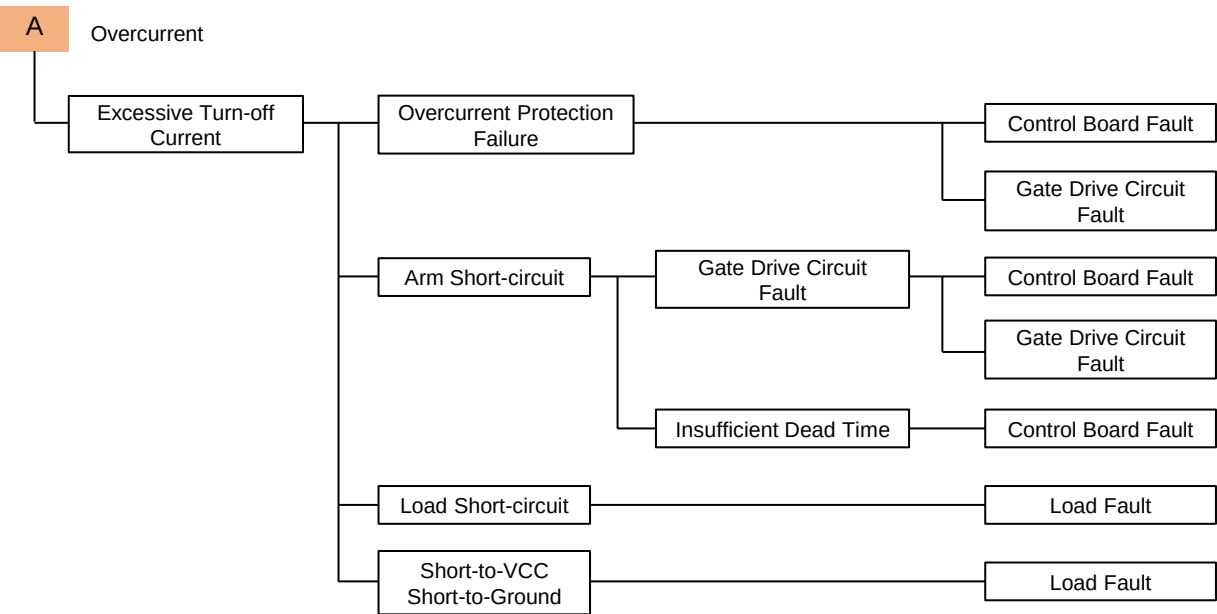


Figure 6.2 Failure Mode A : Overcurrent

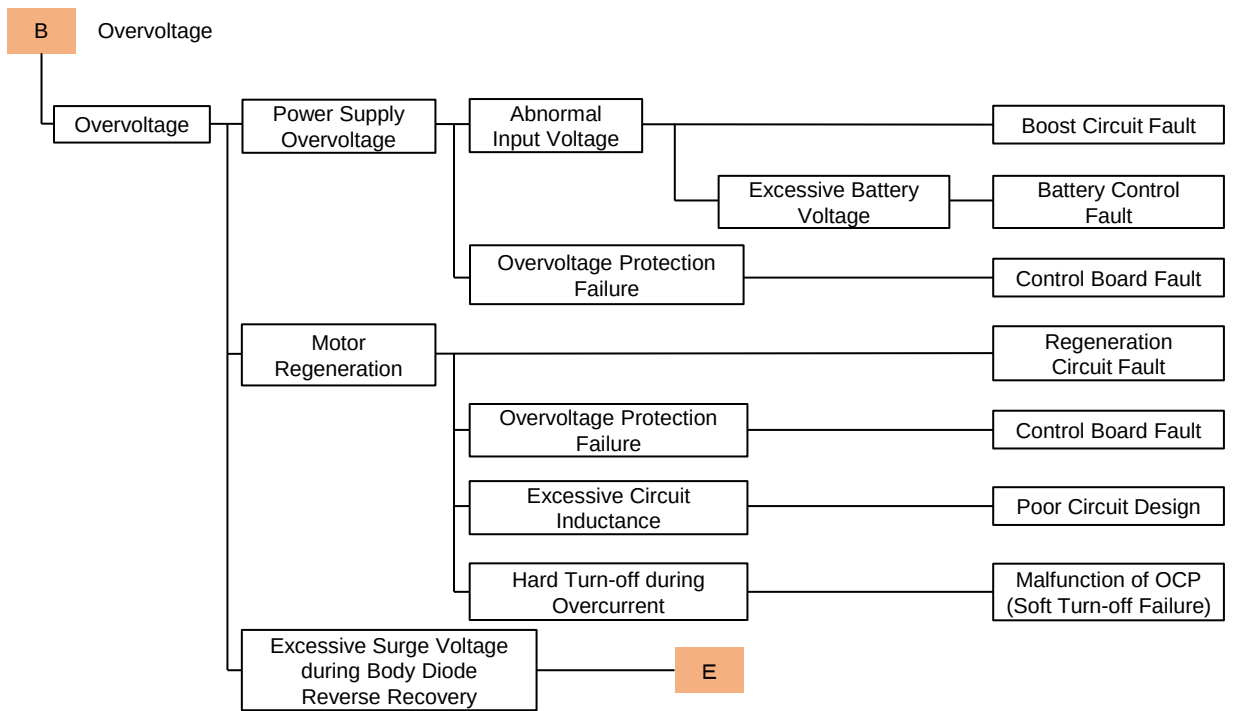


Figure 6.3 Failure Mode B : Overvoltage

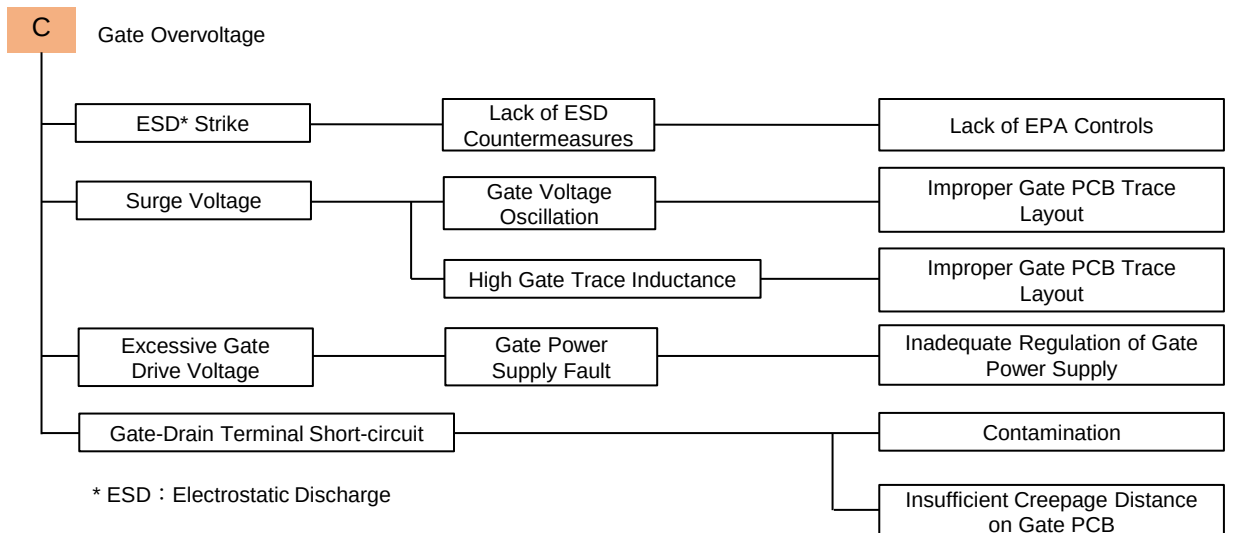
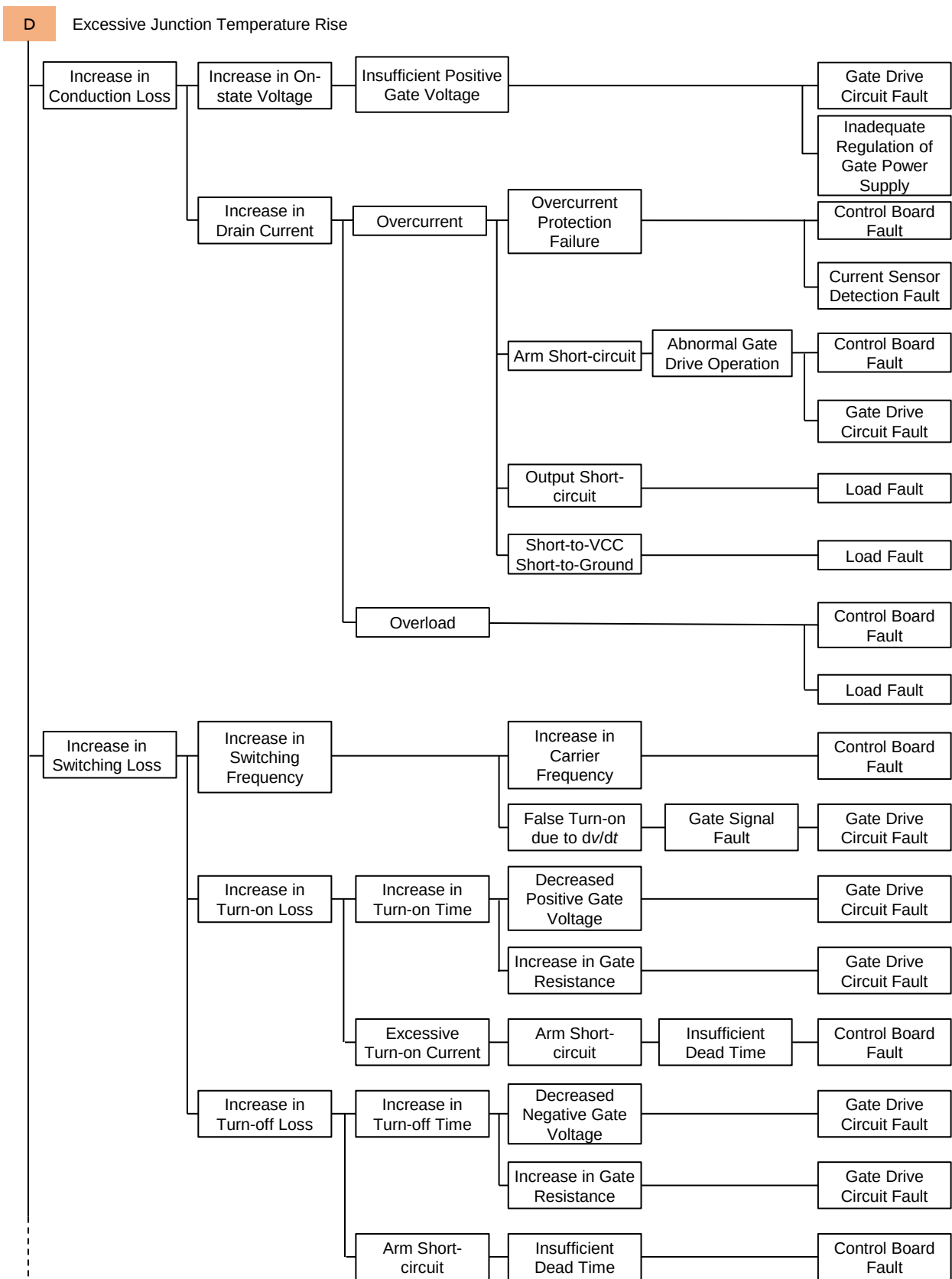


Figure 6.4 Failure Mode C : Gate Overvoltage



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Figure 6.5 Failure Mode D : Excessive Junction Temperature Rise (1)

D : Excessive Junction Temperature Rise (Continued)

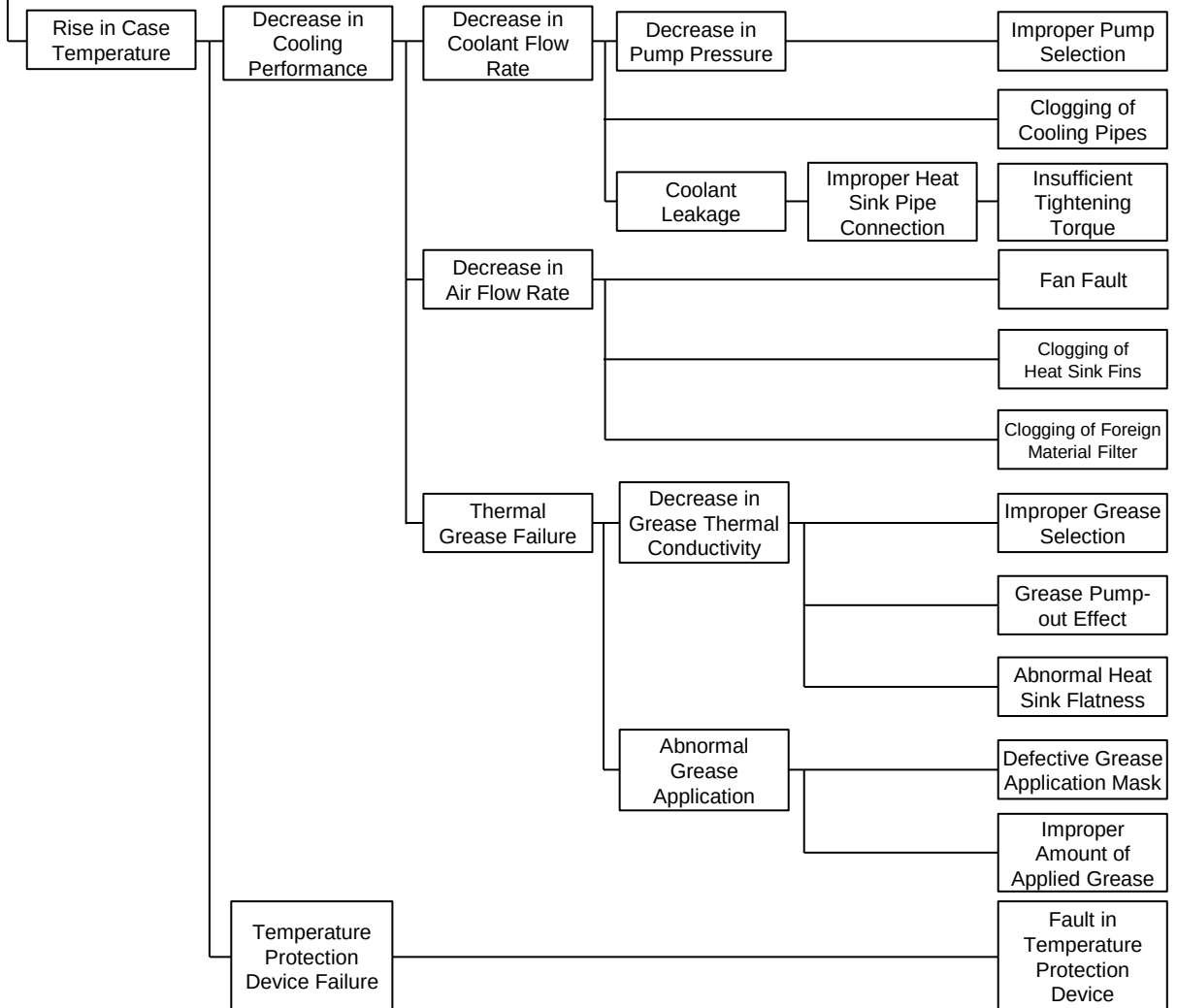


Figure 6.5 Failure Mode D : Excessive Junction Temperature Rise (2)

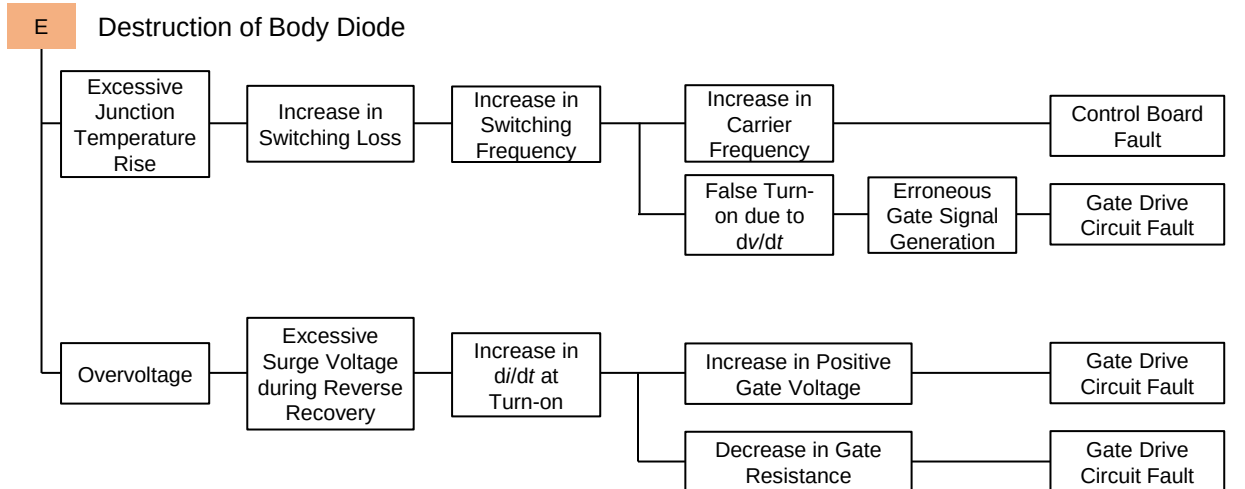
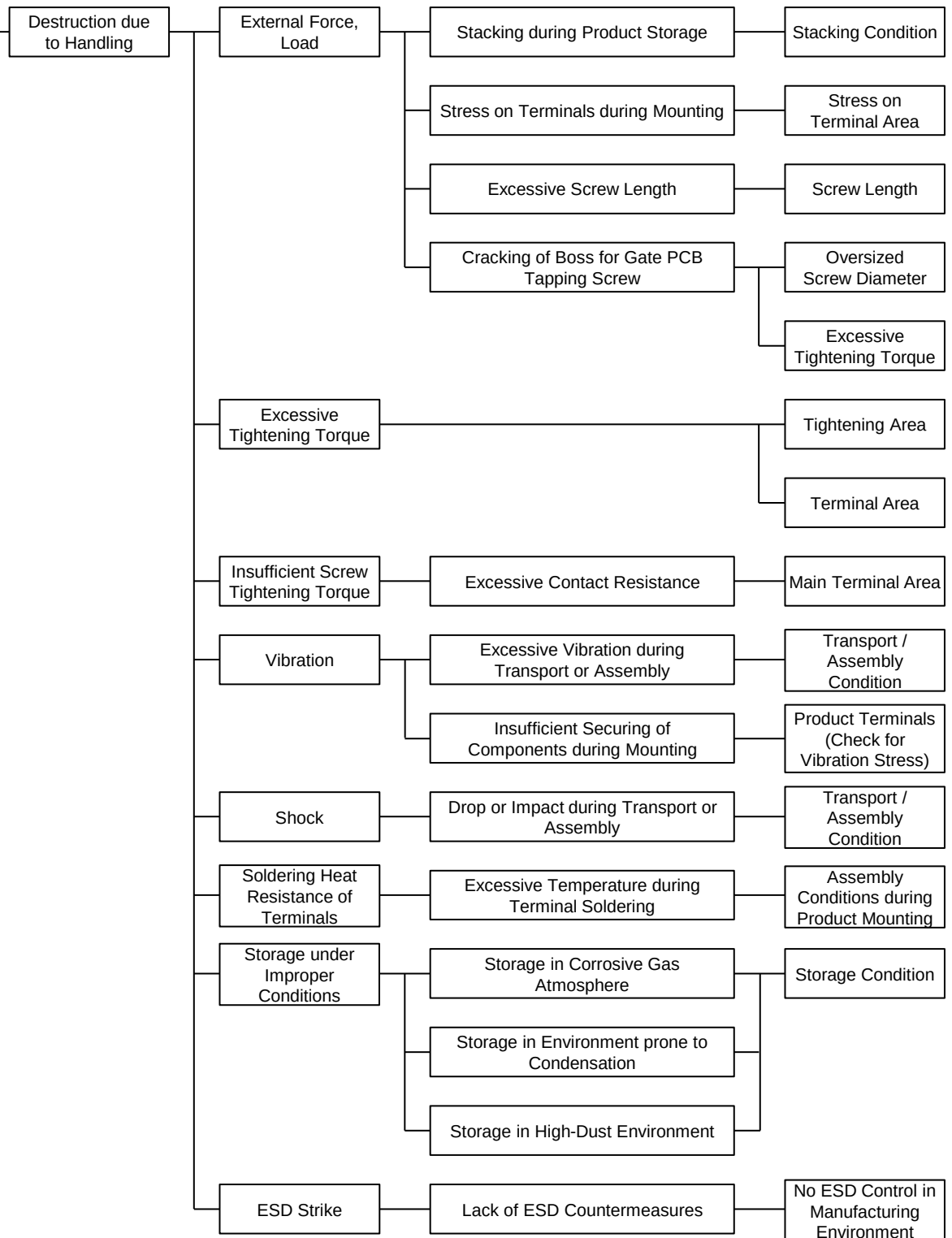


Figure 6.6 Failure Mode E : Destruction of Body Diode

F

Failures related to Reliability and Product Handling



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Figure 6.7 Failure Mode F : Failures Related to Reliability and Product Handling (1)

F : Failures related to Reliability and Product Handling (Continued)

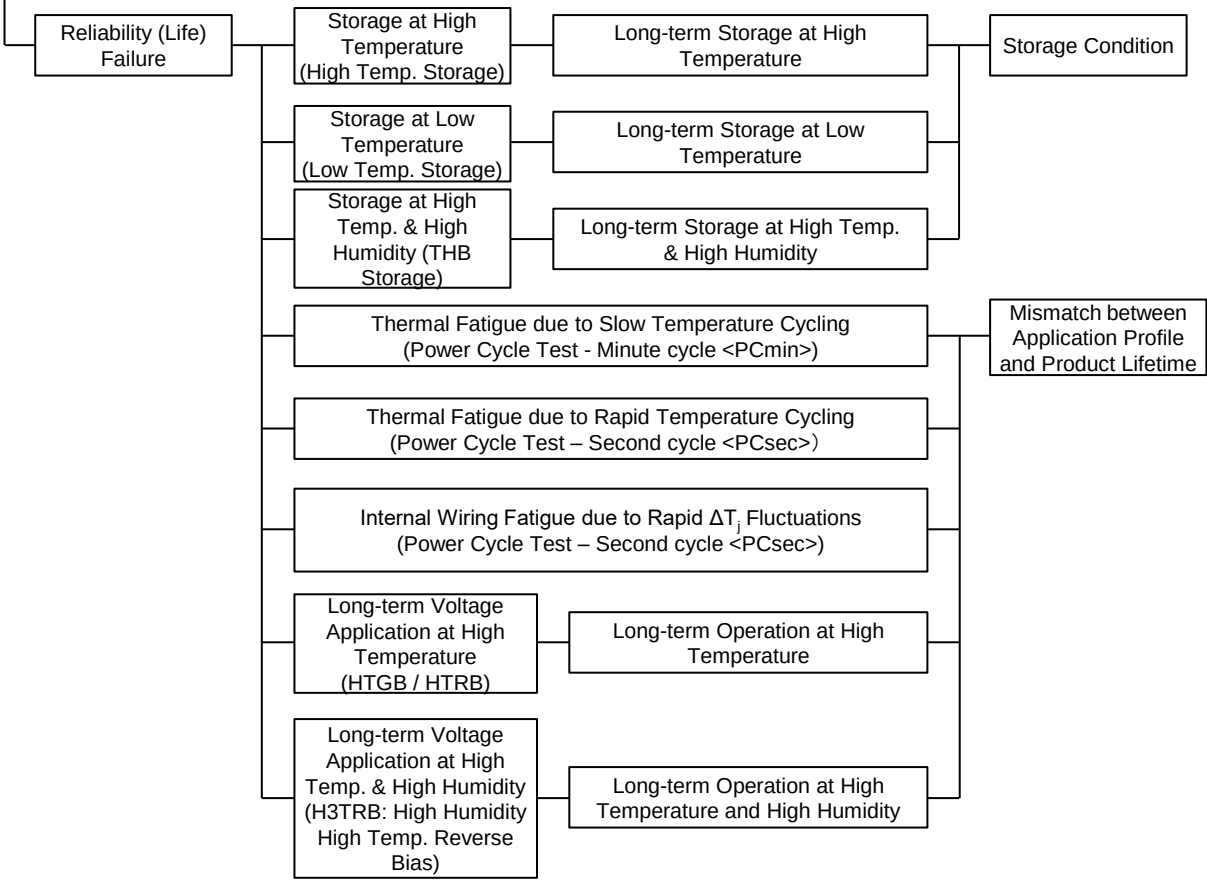


Figure 6.7 Failure Mode F : failures Related to Reliability and Product Handling (2)

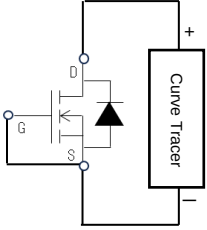
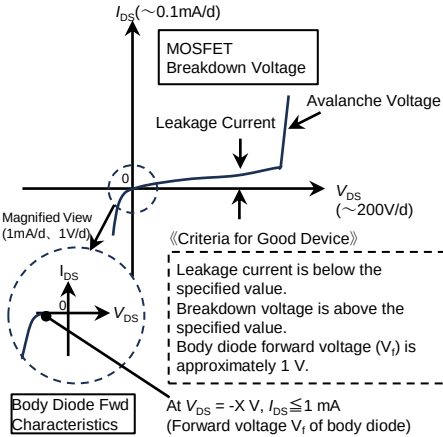
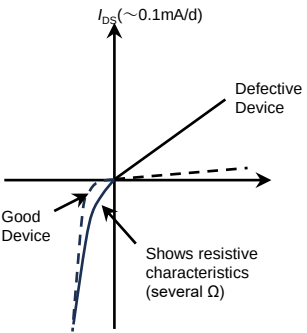
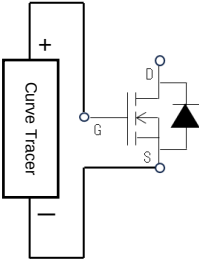
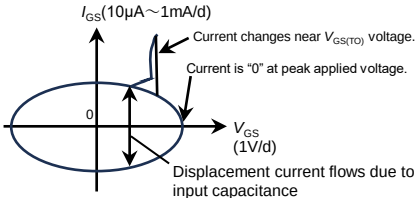
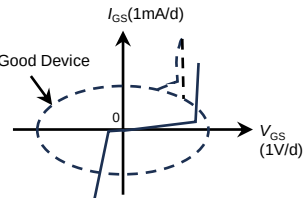
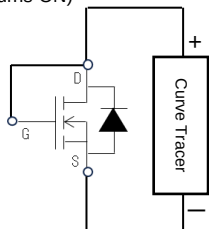
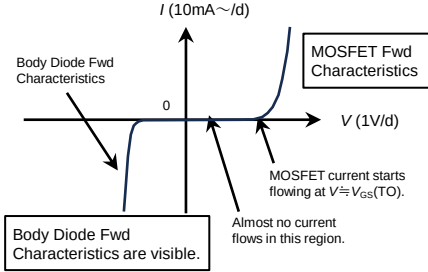
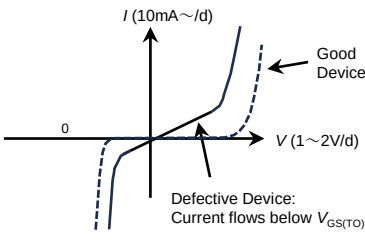
6-2. DEVICE INSPECTION METHOD

This section describes a method to verify the electrical characteristics of SiC-MOSFETs using a semiconductor curve tracer.

The table below presents examples of Pass/Fail criteria based on current and voltage data.

Note: Please be aware that if the device is already degraded or damaged, this method may cause secondary destruction.

TABLE 6.1 Device Characteristic Verification Methods (Reference)

No.	Check Terminals	Curve Tracer Output Waveforms	
		Example: Good Device	Example: Defective Device
1	Between D-S (G-S Short-circuit required) 	 «Criteria for Good Device» - Leakage current is below the specified value. - Breakdown voltage is above the specified value. - Body diode forward voltage (V_f) is approximately 1 V. At $V_{DS} = -X V$, $I_{DS} \leq 1 \text{ mA}$ (Forward voltage V_f of body diode)	 Case: MOSFET Short (Resistive Destruction)
2	Between G-S 	 Case of Good Device (Curve Tracer in AC Mode) «Criteria for Good Device» - Current changes at $V_{GS(TO)}$ voltage. - Current becomes "0" at peak applied voltage. - No leakage current even up to Spec voltage. - Displacement current flows due to input capacitance.	 D-G Short, Degradation of G-S Breakdown Voltage
3	Between D and G-S (Test to verify SiC-MOSFET turns ON) 	 «Criteria for Good Device» - MOSFET current starts flowing at $V \approx V_{GS(TO)}$. - Body diode forward direction (forward voltage) is visible.	 Case: Decrease/Degradation of $V_{GS(TO)}$

- *1. Although this explanation assumes the curve tracer is in AC mode (AC output), please use DC mode (positive or negative voltage output) for observation if necessary. In DC mode, the displacement current is minimized, making it easier to observe leakage-related defects.
- *2. It is difficult to verify the module's isolation voltage or characteristic failures caused by temperature changes using this method.
- *3. While it is possible to check device characteristics using a multimeter (simple tester) with a supply voltage of several volts, it is difficult to "fully assess" the device integrity in this manner.

CHAPTER 7. PRECAUTIONS IN CASE OF ACCIDENTS

7-1. WARNINGS

7-1-1. Warnings Regarding Package Rupture



WARNING

- In the event of a load short-circuit or arm short-circuit, the SiC-MOSFET module must be turned off within a short duration (approximately several μ s). Failure to do so may cause the package to rupture.

This is because the excessive Joule heating generated during a short-circuit rapidly accumulates, exceeding the module's thermal limit and causing catastrophic package rupture. Therefore, please observe the following precautions:

- (1) House the SiC-MOSFET module in a sealed case to prevent injury to personnel in the event of a package rupture.
- (2) Never open the SiC-MOSFET module's closed case while an electric current is being supplied to the module.

7-1-2. Warnings Regarding Burns and Electric Shock



WARNING

- Do not touch or approach the product while it is energized.
There is a risk of burns or electric shock.

7-2. PRECAUTIONS



CAUTION

- Ensure that short-circuit current does not flow for a prolonged period (approximately several hundred μ s) following a failure of the SiC-MOSFET.
There is a risk of smoke generation or fire.

Although the material used for the SiC-MOSFET module's casing resin complies with the UL94V-0 flammability class, please ensure the circuit is protected by a fuse.