8-channel High Voltage analog switch IC

ECN3294TF Product Specification

1. General Description

1.1 General

ECN3294 is an 8-channel High Voltage analog switching IC with bleed resistors on which latch-up free is realized by dielectric isolation technology.

High voltage and low on-resistance MOS switches are used as output devices controlled by a 3.3V or 5.0V signal. The ECN3294 is most suited to ultrasound imaging applications.

1.2 Functions and Features

* High voltage and low on-resistance MOS switches integrated.
* One bleed resistor is built into each switch.
* 8bit shift resister integrated.
* Switch on-resistance: 19 Ω typ. (VPP=100V,VNN=-100V,ISIG=5mA, 25ºC)
* Switch breakdown voltage: 220V
* Power up/down sequence of power supply is free.
* The breed resistance is 17.5kΩ. The customer can arbitrarily select the method of connecting resistance.
* 48-pin LQFP Package. (RoHS compliant)

1.3 Block diagram

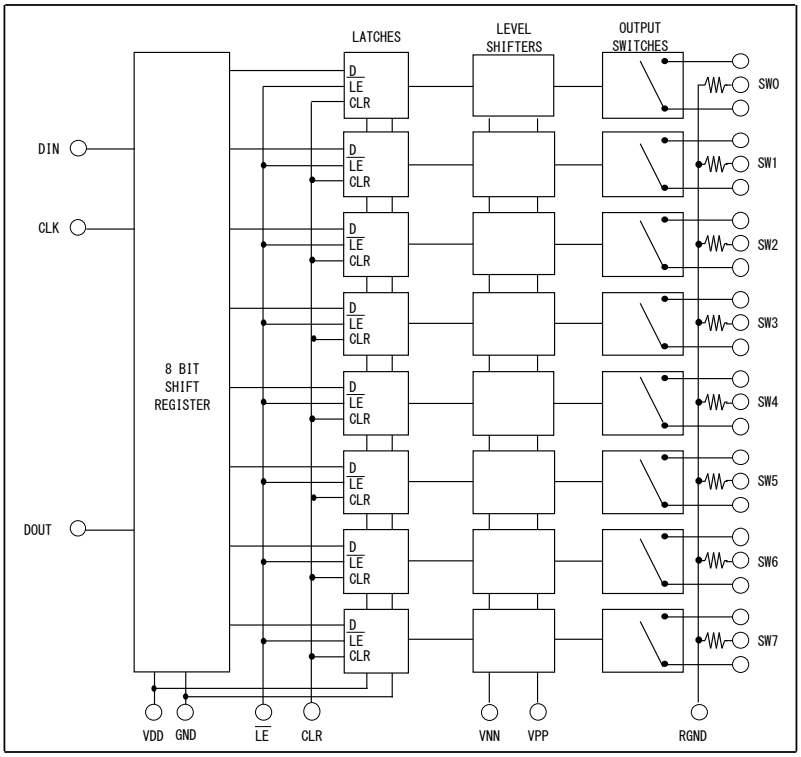


Fig. 1.3.1 Block diagram

2. Specifications

2.1 Absolute Maximum Ratings

Table 2.1.1 Absolute Maximum Ratings

No.	Items	Symbol	Terminal	Values	Unit	Note
1	Logic power supply voltage	VDD	VDD	-0.5 ~ +7.0	V	Ta＝25ºC
2	VPP-VNN supply voltage	-	VPP, VNN	220	V	Ta＝25ºC
3	VPP Positive high voltage supply	VPP	VPP	-0.5 to VNN+200	V	Ta＝25ºC
4	VNN negative high voltage supply	VNN	VNN	-200 to +0.5	V	Ta＝25ºC
5	Logic input voltages	-	DIN, CLK, CL, $\overline{LE}$	-0.5 to VDD+0.3	V	Ta＝25ºC
6	Analog signal range	-	SW0 to SW7	VNN to VPP	V	Ta＝25ºC
7	Bleed Resistor input voltages	-	BR0 to BR7	VNN to VPP	V	Pulse signal
8	Operating junction temperature	Tjop	-	-20 to +125	ºC	
9	Storage temperature	Tstg	-	-65 to +150	ºC	
10	Power dissipation	Pw	-	1.0	W	Ta＝70ºC

2.2 Electrical Characteristics

2.2.1 DC Characteristics

Table 2.2.1 DC Characteristics Ta=25°C VDD=5.0V

No.	Items	Symbol	Spec			Unit	Test conditions	
			Min	Typ	Max			
1	Small signal switch on resistance	RONS	-	24	38	Ω	ISIG=5mA	VPP=40V, VNN=-160V
			-	17	27		ISIG=200mA	
			-	19	27		ISIG=5mA	VPP=100V, VNN=-100V
			-	15	24		ISIG=200mA	
			-	19	25		ISIG=5mA	VPP=160V, VNN=-40V
			-	15	25		ISIG=200mA	
2	Small signal switch on resistance matching	ΔRONS	-	5	20	%	VPP=100V, VNN=-100V ISIG=5mA	
3	Large signal switch on resistance	RONL	-	16	—	Ω	VPP=100V VNN=-100V	ISIG =1A
4	Value of output bleed resistance	RINT	10	17.5	25	kΩ	IRINT=0.5mA, Output switch to RGND	
5	Switch off leakage per switch	ISOL	-	1.0	10	μA	VSIG=VPP-10V, or VNN+10V	
6	DC offset switch (off)	DCOFF	-	10	100	mV	RL=100kΩ	
7	DC offset switch (on)	DCON	-	10	100	mV	RL=100kΩ	
8	Positive HV supply current	IPPQ1	-	10	50	μA	All SWs off	
9	Negative HV supply current	INNQ1	-	-10	-50	μA	All SWs off	
10	Positive HV supply current	IPPQ2	-	10	50	μA	All SWs on, ISIG=5mA	
11	Negative HV supply current	INNQ2	-	-10	-50	μA	All SWs on, ISIG=5mA	
12	IPP Supply current	IPP	-	-	7.0	mA	VPP=40V VNN=-160V	fSW=50kHz no-load
			-	-	5.0		VPP=100V VNN=-100V	
			-	-	5.0		VPP=160V VNN=-40V	
13	INN Supply current	INN	-	-	7.0	mA	VPP=40V VNN=-160V	fSW=50kHz no-load
			-	-	5.0		VPP=100V VNN=-100V	
			-	-	5.0		VPP=160V VNN=-40V	
14	Logic supply average current	IDD	-	-	4.0	mA	fCLK=5MHz	
15	Logic supply quiescent current	IDDQ	-	-	10	μA		
16	Data out source current	ISOR	0.45	0.70	-	mA	Vdout=VDD-0.7V	
17	Data out sink current	ISINK	0.45	0.70	-	mA	Vdout=0.7V	

2.2.2 AC Characteristics

Table 2.2.2 AC Characteristics Ta=25°C VDD=5.0V

No.	Items	Symbol	Spec			Unit	Test conditions
			Min	Typ	Max		
1	SW Turn on time	tON	-	-	5.0	μs	VSIG=VPP-10V, RL=10kΩ
2	SW Turn off time	tOFF	-	-	5.0	μs	VSIG=VPP-10V, RL=10kΩ
3	Clock frequency	fCLK	-	-	20	MHz	50% duty cycle, fDIN=fCLK/2 VDD=3.0V or 5.0V
4	Clock delay time to data out	tDO	30	-	110	ns	DOUT terminal, VDD=3.0V
			20	-	70	ns	DOUT terminal, VDD=5.0V
5	Output voltage spike	+VSPK	-	-	150	mV	VPP=40V, VNN=-160V, RL=50Ω
		-VSPK	-	-	-200		
		+VSPK	-	-	150		VPP=100V, VNN=-100V, RL=50Ω
		-VSPK	-	-	-200		
		+VSPK	-	-	150		VPP=160V, VNN=-40V, RL=50Ω
		-VSPK	-	-	-200		

2.2.3 AC Characteristics (for reference purpose only)

These items are not tested when shipped.

Table 2.2.3 AC Characteristics (for reference purpose only) Ta=25°C VDD=5.0V

No.	Items	Symbol	Spec			Unit	Condition
			Min	Typ	Max		
1	Off capacitance SW to GND	CSG (off)	-	9	-	pF	Measurement signal (DC 0V, AC 1MHz)
2	On Capacitance SW to GND	CSG (on)	-	14	-	pF	Measurement signal (DC 0V, AC 1MHz)
3	SW off isolation	KO	-30	-33	–	dB	f=5MHz, RL=1kΩ//15pF
			-54	-60	–	dB	f=5MHz, RL=50Ω
4	SW crosstalk	KCR	-54	-60	–	dB	f=5MHz, RL=50Ω

3. Recommended Operating Conditions

Please operate in use within the limit of recommended operating conditions detailed in Table 3.1.

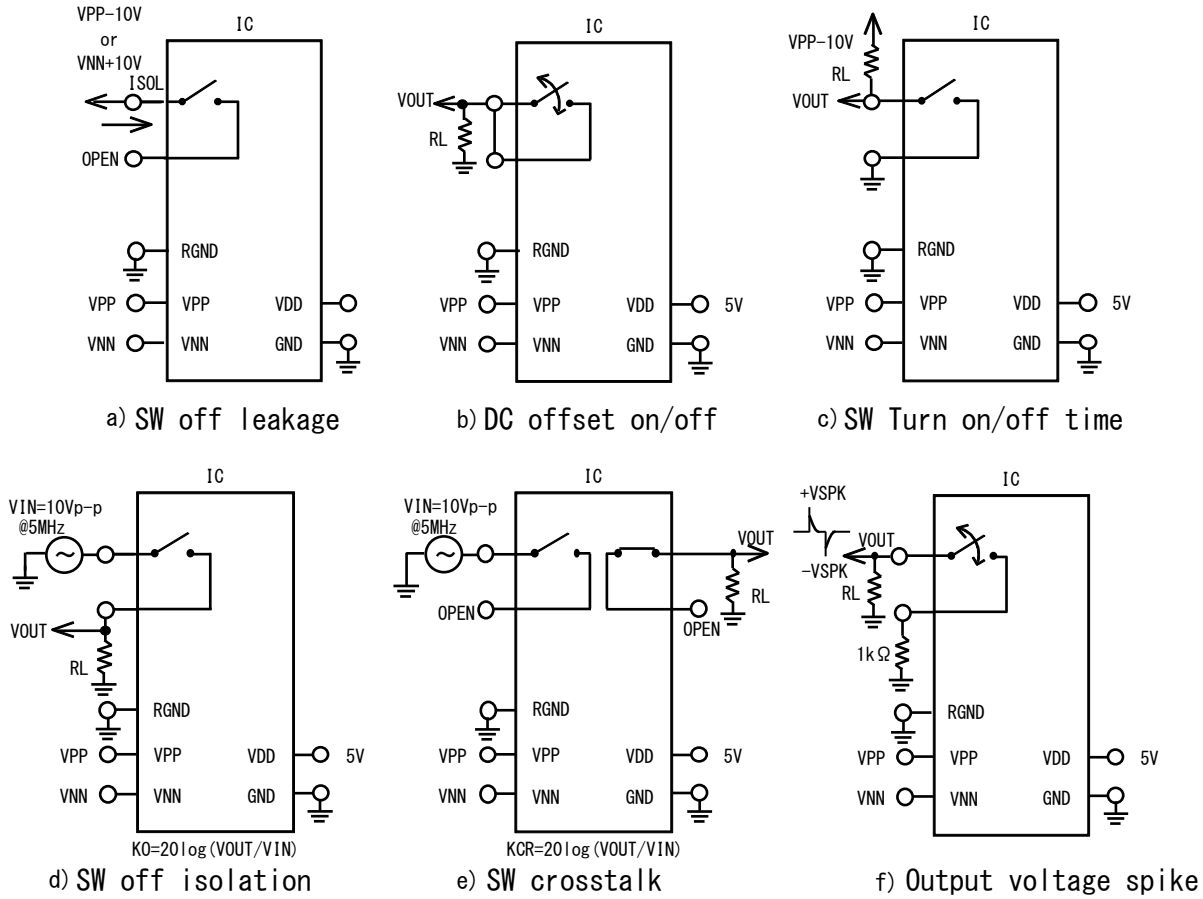
Table 3.1 Recommended Operating Conditions

No	Items	Symbol	Recommended Value	Unit	Condition
1	Logic power supply voltage	VDD	3.0 to 5.5	V	
2	Positive high voltage supply	VPP	40 to VNN+200	V	
3	Negative high voltage supply	VNN	-160 to -40	V	
4	High-level input voltage	VIH	0.9VDD to VDD	V	
5	Low-level input voltage	VIL	0 to 0.1VDD	V	
6	Analog signal voltage peak to peak	VSIG	VNN+10 to VPP-10	V	
7	Operating free air-temperature	Ta	0 to 70	^{o}C	
8	Switching frequency	fSW	50 max	kHz	Duty Cycle=50%
9	Set up time for $\overline{LE}$	tSD	Min.75	ns	
10	Pulse width of $\overline{LE}$	tWLE	Min.75	ns	
11	Time width of CL	tWCL	Min.60	ns	
12	Set up time DATA to Clock	tSU	Min.10	ns	
13	Hold time DATA from Clock	th	Min.20	ns	
14	Maximum VSIG Slew Rate	dV/dt	Max.30	V/ ns	

Attention ;

1) Power on/off sequence of power supply is arbitrary except GND terminal of IC must be powered-up first and powered-down last.
2) It is indispensable to make there are not to exceed a maximum rated voltage by the occurrence of the excessive voltage in case of power-on and power-off of the power supply.

4. Test Circuit



Note : The bleed resistor is assumed to be a condition not connected. The terminal BR (BR0-BR7) is assumed to be open.

Fig. 4.1 Test Circuit

5. Timing Waveforms

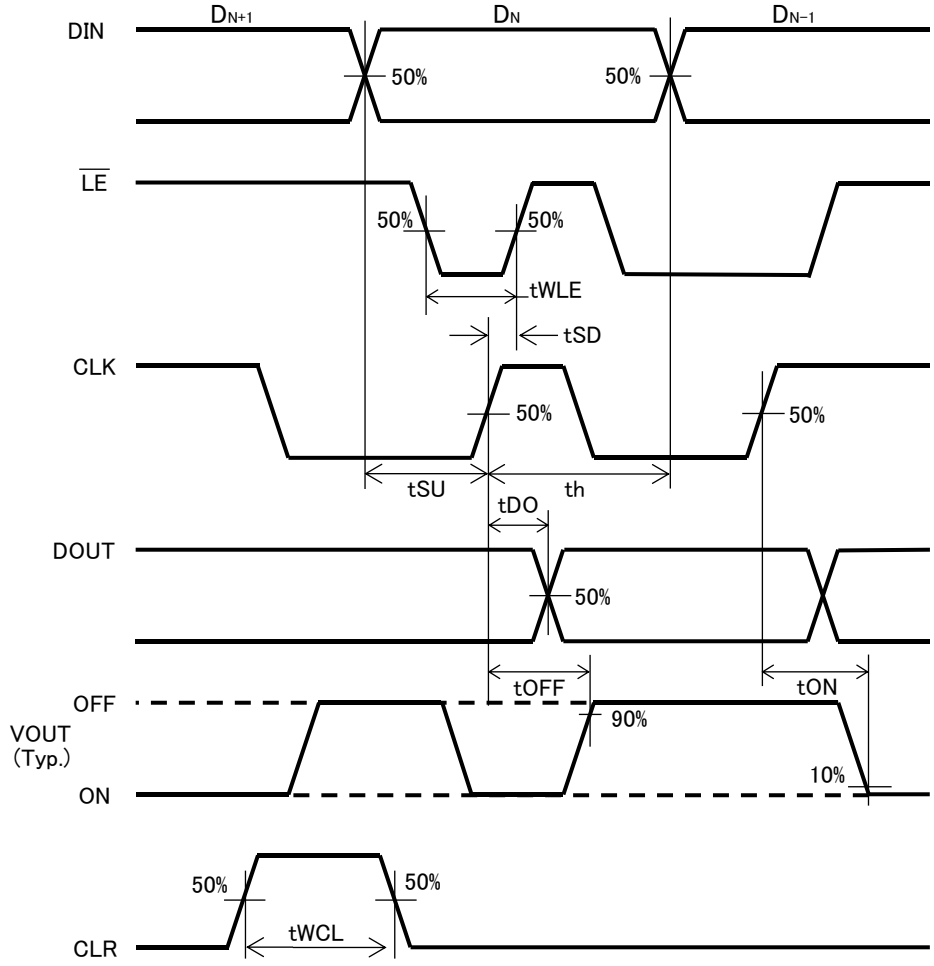


Fig. 5.1 Timing Waveforms

Note

1. Serial data is clocked in on the rising edge of CLK.

2. The switches go to a state retaining their present condition on the rising edge of $\overline{LE}$.

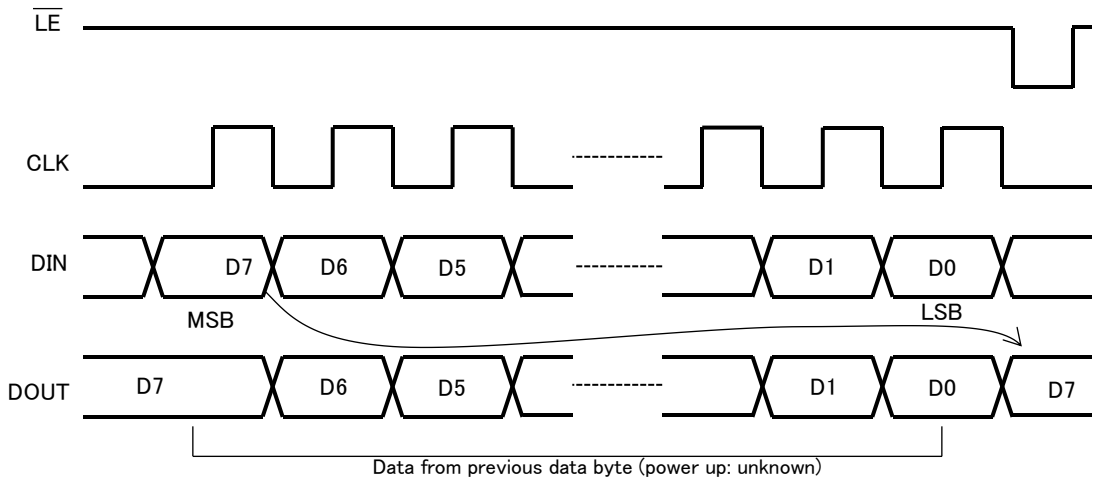


Fig. 5.2 LATCH ENABLE Timing Waveforms

6. Truth Table

Table 6.1 Truth table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

X = Don't care

Note

1. The 8 Switches operate independently.

2. When $\overline{LE}$ is low, the shift register data flows through the latch.

3. Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

4. When switch 7 is ON, DOUT is high.

5. The clear input overrides all other inputs.

7. Pin Function

ECN3294TF LQFP48（48Pin LQFP）

Table 7.1. Pin Function

Pin	Name	Functions	Note
1	SW5	Analog Switch 5	
2	N/C	No connection	*1
3	SW4	Analog Switch 4	
4	BR4	Bleed resistor 4	
5	SW4	Analog Switch 4	
6	N/C	No connection	*1
7	N/C	No connection	*1
8	SW3	Analog Switch 3	
9	BR3	Bleed resistor 3	
10	SW3	Analog Switch 3	
11	N/C	No connection	*1
12	SW2	Analog Switch 2	
13	BR2	Bleed resistor 2	
14	SW2	Analog Switch 2	
15	N/C	No connection	*1
16	SW1	Analog Switch 1	
17	BR1	Bleed resistor 1	
18	SW1	Analog Switch 1	
19	N/C	No connection	*1
20	SW0	Analog Switch 0	
21	BR0	Bleed resistor 0	
22	SW0	Analog Switch 0	
23	N/C	No connection	*1
24	VPP	Positive High Voltage Supply	*2
25	VNN	Negative High Voltage Supply	*2
26	N/C	No connection	*1
27	RGND	Ground. Connect to Bleed Resister.	
28	GND	Ground	
29	VDD	Logic Supply Voltage	
30	N/C	No connection	*1
31	N/C	No connection	*1
32	N/C	No connection	*1
33	DIN	Serial Data Input	
34	CLK	Serial Clock Input	
35	$\overline{LE}$	Latch-Enable Input	
36	CLR	Latch-Clear Input	
37	DOUT	Serial Data Output	
38	N/C	No connection	*1
39	SW7	Analog Switch 7	
40	BR7	Bleed resistor 7	
41	SW7	Analog Switch 7	
42	N/C	No connection	*1
43	SW6	Analog Switch 6	
44	BR6	Bleed resistor 6	
45	SW6	Analog Switch 6	
46	N/C	No connection	*1
47	SW5	Analog Switch 5	
48	BR5	Bleed resistor 5	

Note *1. NOT connected on chip internal.*
2. High voltage supply.

8. Pin configuration

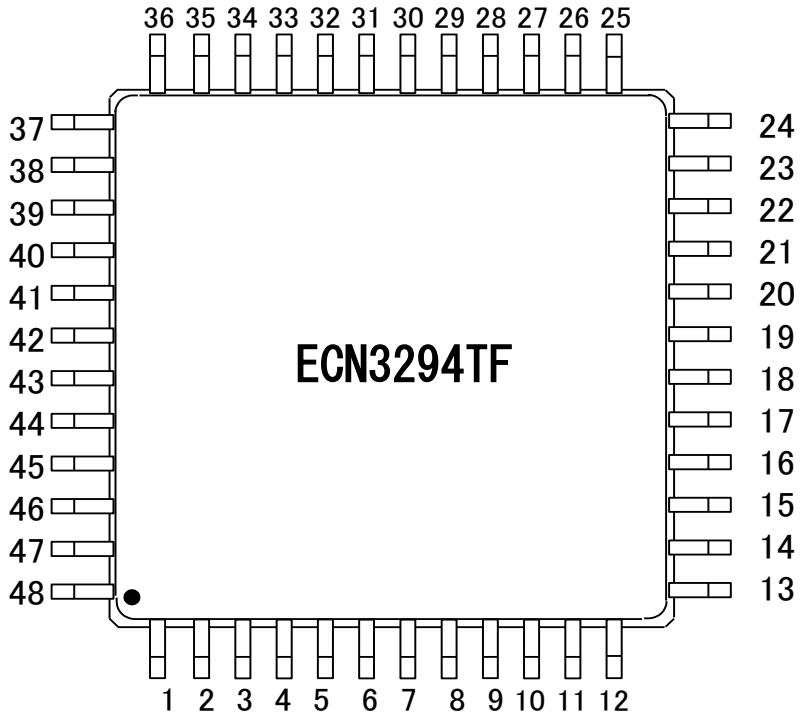


Fig. 8.1 Pin configuration(Top view)

9. Inspection

Hundred percent inspections shall be conducted on electric characteristics.

10. Precautions for use

In this document, “MPSD” stands for Minebea Power Semiconductor Device Inc.

10.1 Countermeasures against Electrostatic Discharge (ESD)

(a) Customers need to take precautions to protect ICs from electrostatic discharge (ESD). The material of the container or any other device used to carry ICs should be free from ESD, which can be caused by vibration during transportation. Use of electrically conductive containers is recommended as an effective countermeasure.
(b) Everything that touches ICs, such as the work platform, machine, measuring equipment, and test equipment, should be grounded.
(c) Workers should be high-impedance grounded (100kΩ to 1MΩ) while working with ICs, to avoid damaging the ICs by ESD.
(d) Friction with other materials, such as high polymers, should be avoided.
(e) When carrying a PCB with a mounted IC, ensure that the electric potential is maintained at a constant level using the short-circuit terminals and that there is no vibration or friction.
(f) The humidity at an assembly line where ICs are mounted on circuit boards should be kept around 45 to 75 percent using humidifiers or such. If the humidity cannot be controlled effectively, using ionized air blowers (ionizers) is effective.

10.2 Output Short-circuit Protection

The MPSD IC could break by a short circuit (ex. load short). Therefore, external protection is needed.

10.3 Maximum Ratings

Regardless of changes in external conditions during use of the MPSD IC, the “maximum ratings” described in this document should never be exceeded when designing electronic circuits that employ the MPSD IC. If maximum ratings are exceeded, the MPSD IC may be damaged or destroyed. In no event shall MPSD be liable for any failure in the MPSD IC or any secondary damage resulting from use at a value exceeding the maximum ratings.

10.4 Derating Design

Continuous high-load operation (high temperatures, high voltages, large currents) should be avoided and derating design should be applied, even within the ranges of the maximum ratings, to ensure reliability.

10.5 Safe Design

The MPSD IC may fail due to accidents or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy and measures to prevent misuse, in order to avoid extensive damage in the event of a failure.

10.6 Application

If the MPSD IC is applied to the following uses where high reliability is required, obtain the document of permission from MPSD in advance.

・Automobile, Train, Vessel, etc.

Do not apply the MPSD IC to the following uses where extremely high reliability is required.

・Nuclear power control system, Aerospace instrument, Life-support-related medical equipment, etc.

10.7 Soldering

Lead-free solder is used for coating pins and the tab of this IC.
Refer to ”Instructions for Use of High-Voltage Monolithic ICs” for soldering conditions.

10.8 Storage Conditions

(1) Before opening the moisture prevention bag (aluminum laminate bag)
Temperature: less than 40˚C
Humidity: less than 90%RH
Period: less than 12 months

(2) After opening the moisture prevention bag (aluminum laminate bag)
Temperature: 5˚C to 30˚C
Humidity: less than 60%RH
Period: less than 168 hours

※ When the period of (1) and (2) is likely to expire, store the IC in a drying furnace (10%RH or lower) at ordinary temperature.

(3) Baking process
When the period of (1) and (2) has expired, the IC should be baked in accordance with the following conditions. (However, when the IC is stored in a drying furnace (10%RH or lower) ordinary temperature, there is no need to bake.) Do not bake the tape and the reel of the taping package because they are not heat resistant. Transfer the IC to a heat resistant container prior to baking.
Temperature: 125˚C to 135˚C
Period: more than 48 hours

10.9 Others

See “Instructions for Use of High-Voltage Monolithic ICs ” for other precautions and instructions on how to deal with these kinds of products.

11. Usage

(1) MPSD warrants that the MPSD products have the specified performance according to the respective specifications at the time of its sale. Testing and other quality control techniques of the MPSD products by MPSD are utilized to the extent MPSD needs to meet the specifications described in this document. Not every device of the MPSD products is specifically tested on all parameters, except those mandated by relevant laws and/or regulations.

(2) Following any claim regarding the failure of a product to meet the performance described in this document made within one month of product delivery, all the products in relevant lot(s) shall be re-tested and re-delivered. The MPSD products delivered more than one month before such a claim shall not be counted for such response.

(3) MPSD assumes no obligation nor makes any promise of compensation for any fault which should be found in a customer's goods incorporating the products in the market. If a product failure occurs for reasons obviously attributable to MPSD and a claim is made within six months of product delivery, MPSD shall offer free replacement or payment of compensation. The maximum compensation shall be the amount paid for the products, and MPSD shall not assume responsibility for any other compensation.

(4) MPSD reserves the right to make changes in this document and to discontinue mass production of the relevant products without notice. Customers are advised to confirm specification of the product of inquiry before purchasing of the products that the customer desired. Customers are further advised to confirm before purchasing of such above products that the product of inquiry is the latest version and that the relevant product is in mass production status if the purchasing of the products by the customer is suspended for one year or more.

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When exporting, re-export transshipping or otherwise transferring the MPSD products (technologies) and END Products, all necessary procedures are to be taken in accordance with Foreign Exchange and Foreign Trade Act (Foreign Exchange Act) of Japan, Export Administration Regulations (EAR) of US, and any other applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdictions over the parties or transaction.

◆Appendix-Supplementary Data

1. Package Outline

Units : mm

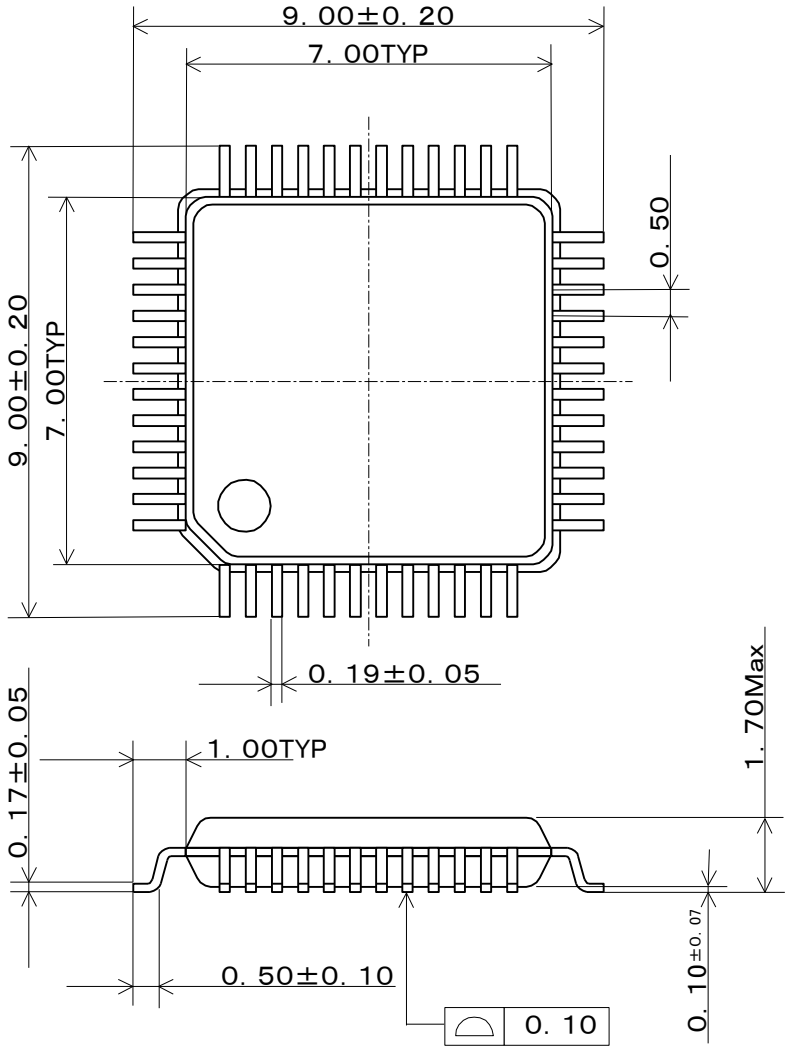


Fig.A Package outline

2. Marking spec

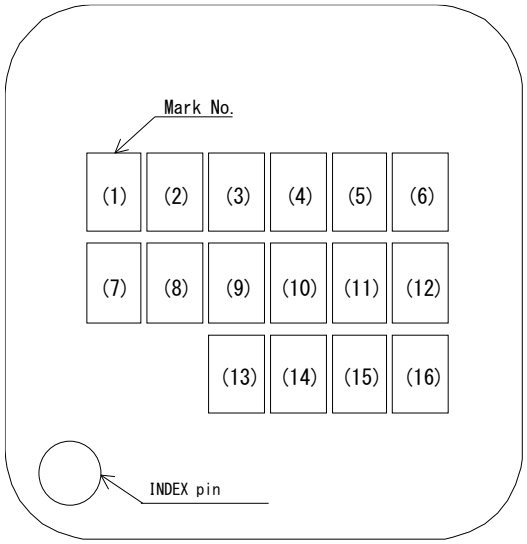


Fig.B Marking

1) No.(1) ; Blank

2) No.(2)～(6) ; Manufacturing No.
No.(2) ; Year code (Least significant digit of Assembled year (A.D.))
No.(3) ; Month code (Refer to below.)
Jan. ; A, Feb. ; B, Mar. ; C, Apr, ; D,
May ; E, June ; K, July ; L, Aug. ; M,
Sep. ; N, Oct. ; X, Nov. ; Y, Dec. ; Z
No.(4)～(6) ; Serial number

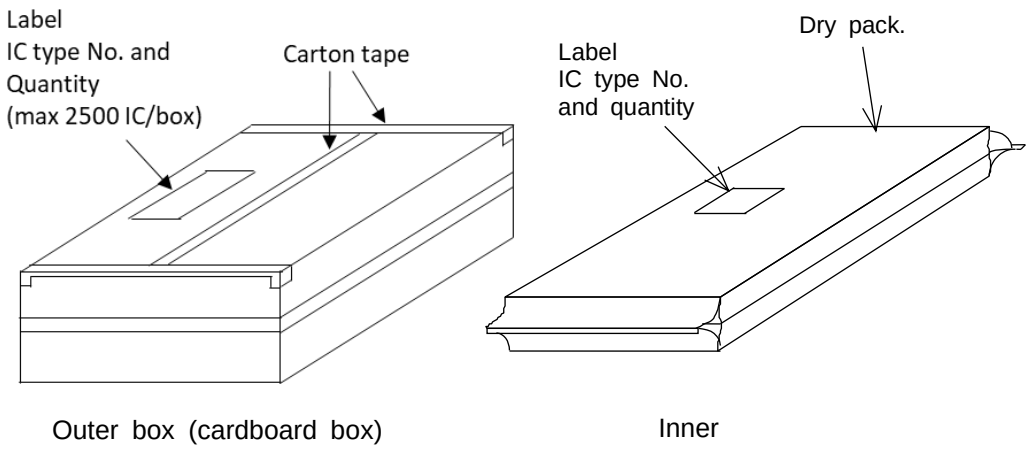
3) No.(7) ; Blank

4) No.(8)～(16) ; Product name ; ECN3294TF

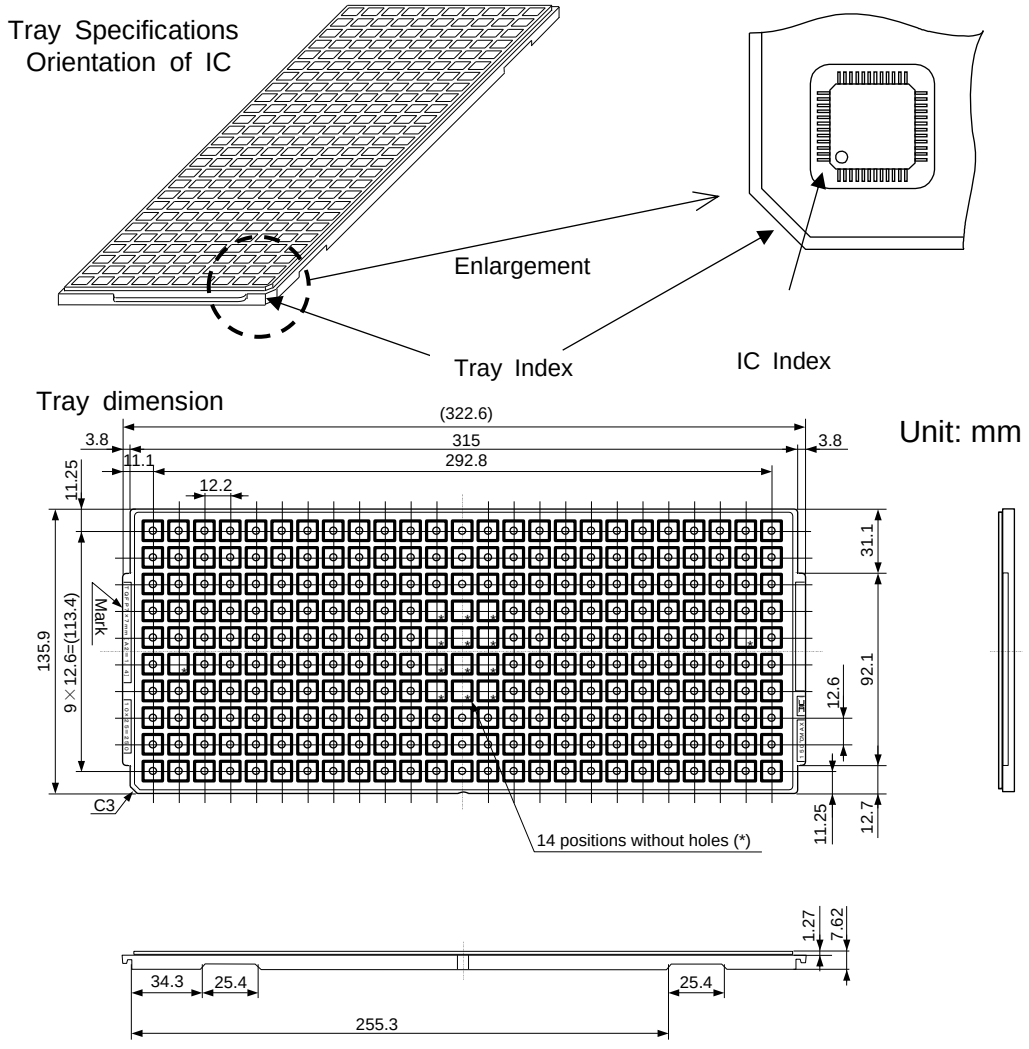
3. Packing Form

Packaging details are as shown below. Order quantities are basically multiples of 2500.

1.Outer and inner packing



2.Tray



(1) Material of tray is PPE containing carbon and static proof.
(2) Packing quantity is max 250 IC/Tray.
(3) Maximum heat resistant temperature is 150deg.

Fig.C IC packing detail